EE 505

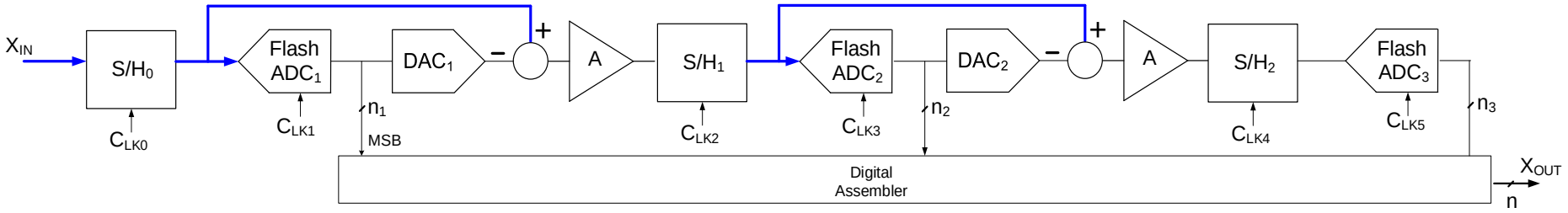
Lecture 23

ADC Design

– Pipeline

Review from last lecture

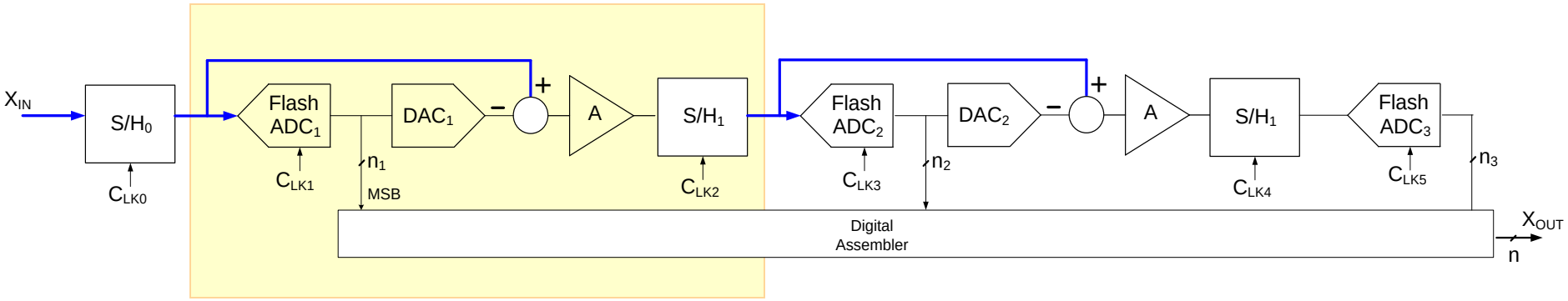
Three-Step Flash ADC with Interstage Gain and S/H



- S/H frees first stage to take another sample during second stage conversion
- This has a pipelining capability
- The pipelined approach dramatically improves speed (close to Flash)
- Significantly reduces the number of comparators
- Introduces latency but not of concern in most applications

Review from last lecture

Three-Step Flash ADC with Interstage Gain

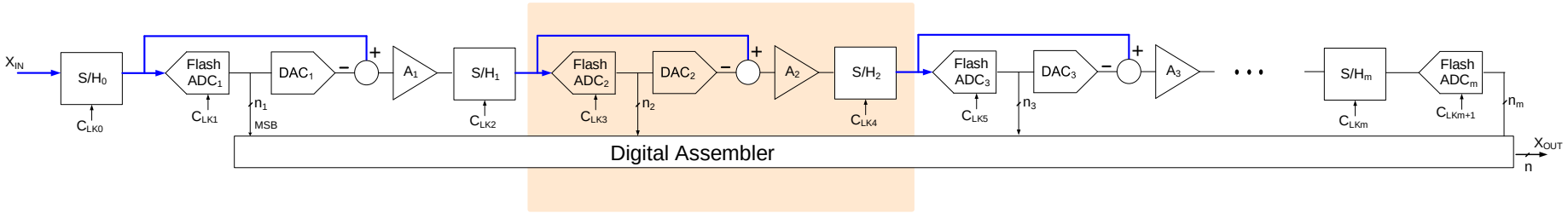


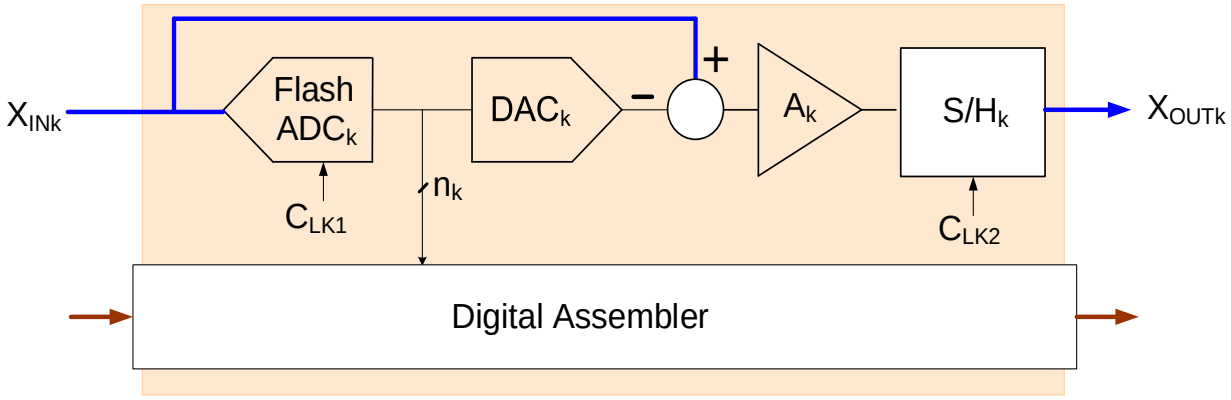
Can be extended to more than 3 stages

- Can go up to 16 bits or maybe a little higher
- Could be as few as one comparator in each Flash ADC
- Further reduction in number of comparators
  (e.g. if one comparator per stage, need only n comparators)
- More latency with more stages but still seldom of concern
- If gains are large enough, comparator offsets in later states can be large
- Will show that with minor modifications, comparator offsets can even be large in first stage

Review from last lecture

Pipelined ADC

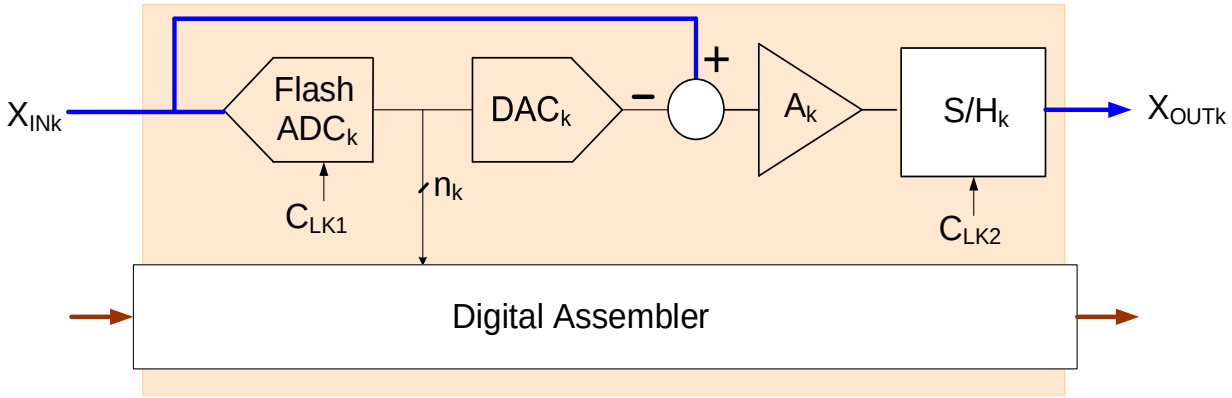




Pipeline Stage

Review from last lecture

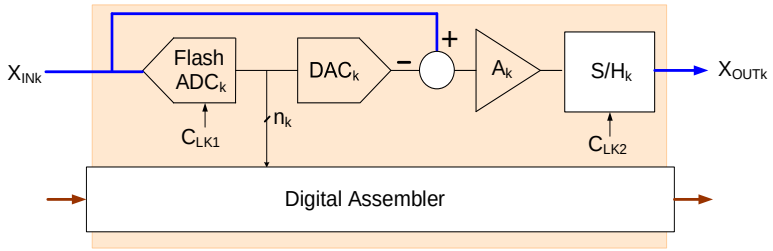
Pipeline Stage



- Appears to be lots of complexity
- S/H is sampling a near-static signal on all stages (except stage 0)
- Ideally the stage gain is chosen so that the maximum signal level at the output is V_{REF} for each stage
- Dominant source of power dissipation is typically the amplifier

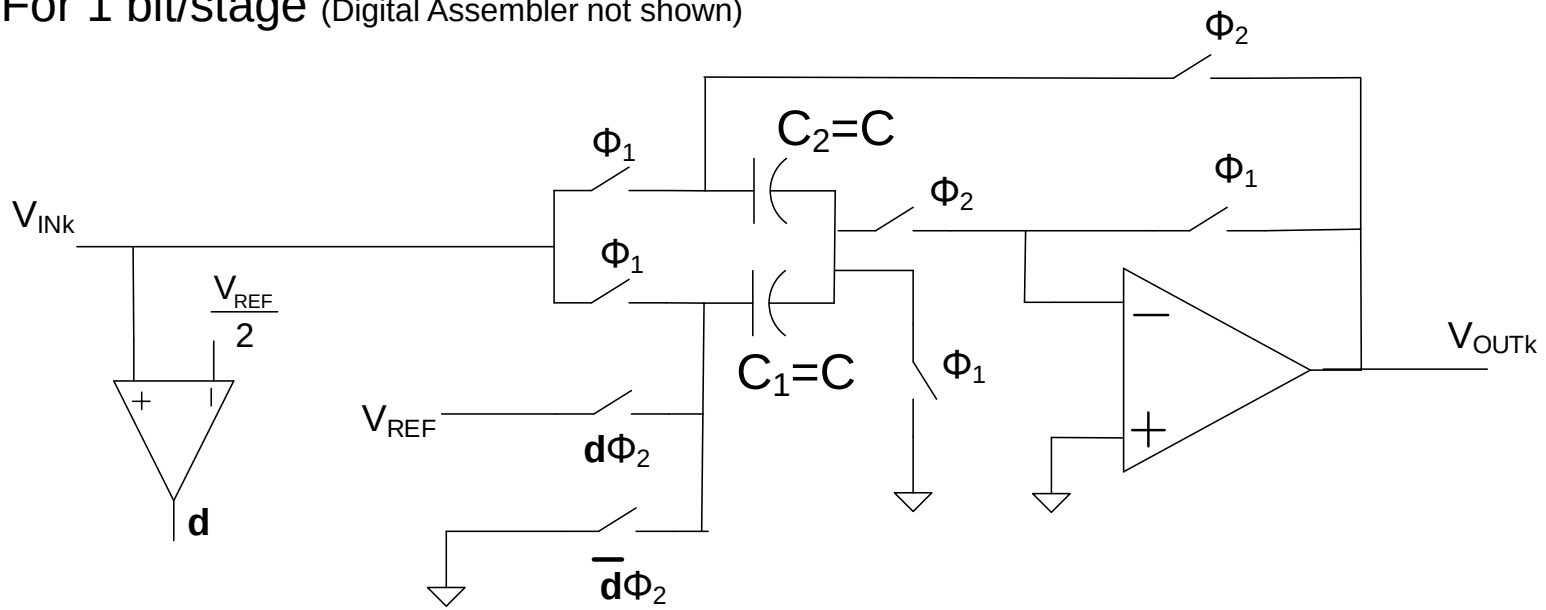
Review from last lecture

Typical SC Pipeline Stage



Very simple and compact stages are used

For 1 bit/stage (Digital Assembler not shown)

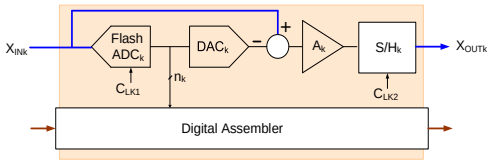


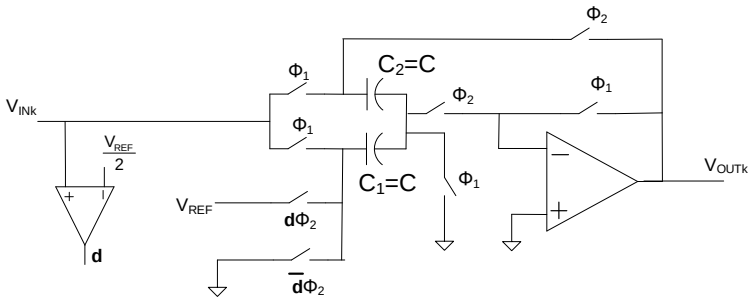
Gain =2

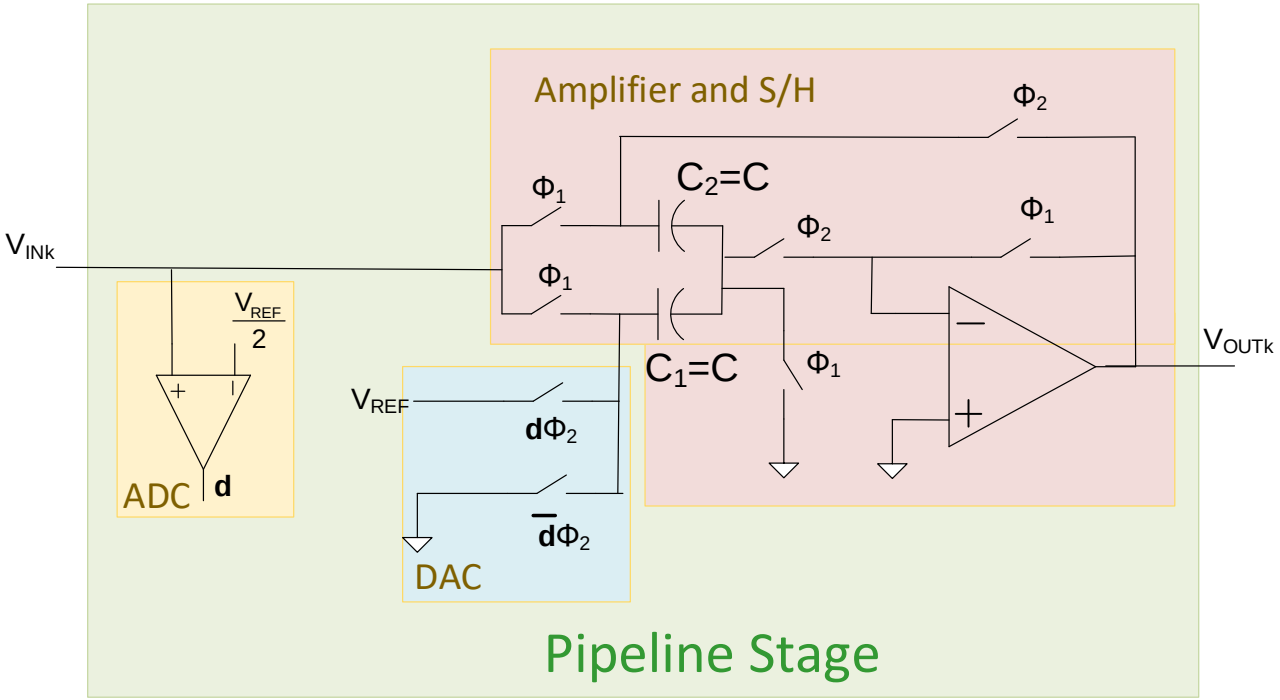
$$V_{OUT}=V_{IN}\left(1+\frac{C_1}{C_2}\right)-d\left(\frac{C_1}{C_2}\right)V_{REF} \quad \Rightarrow \quad V_{OUTk}=2V_{INk}-dV_{REF}$$

Typical SC Pipeline Stage

For 1 bit/stage (Digital Assembler not shown)

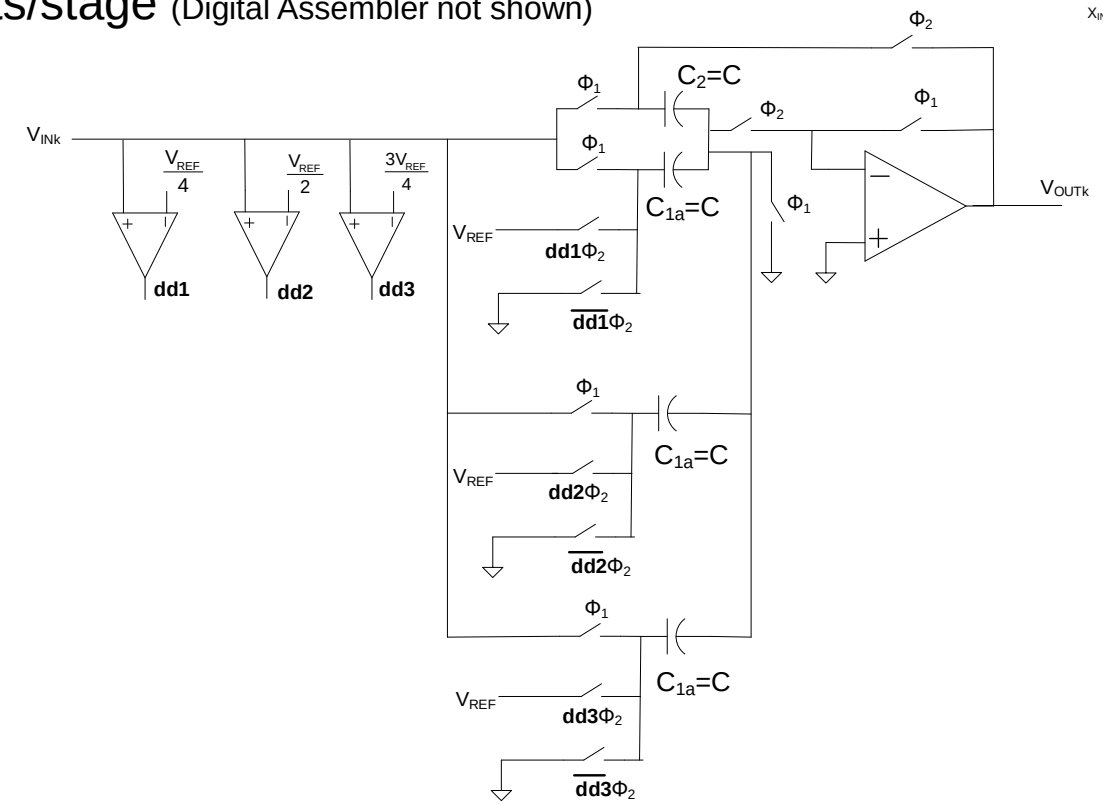


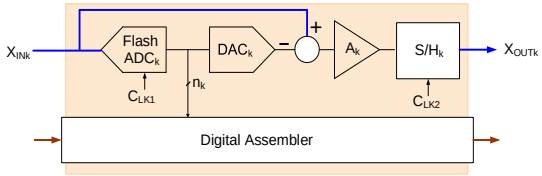




Typical SC Pipeline Stage

For 2 bits/stage (Digital Assembler not shown)





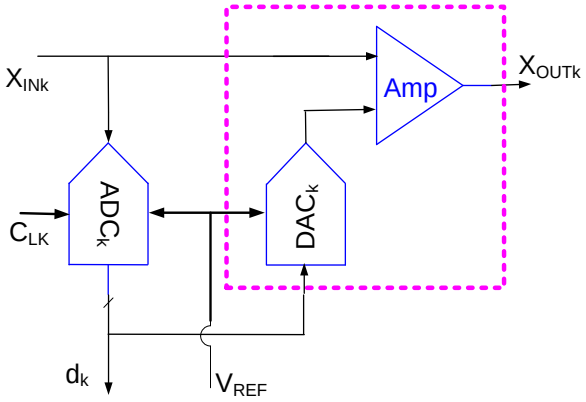
Gain =4

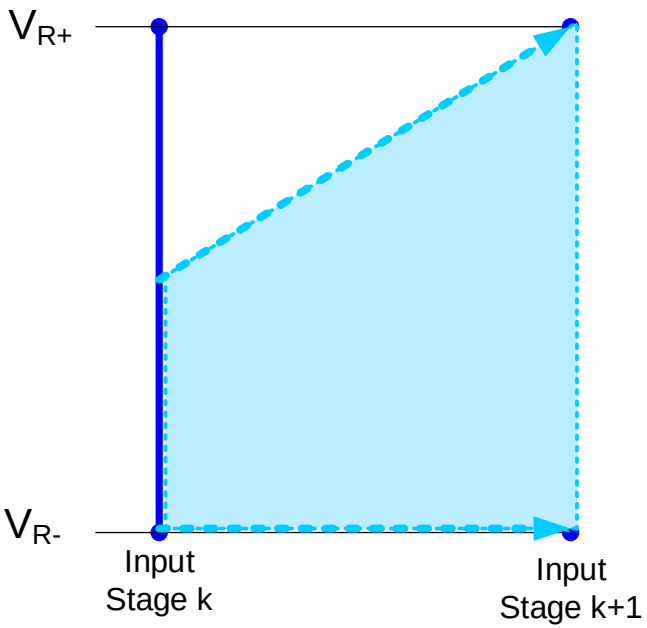
$$V_{OUT}=V_{IN}\left(1+\frac{C_{1a}+C_{1b}+C_{1c}}{C_2}\right)-\left(d_{d1}\left(\frac{C_{1a}}{C_2}\right)+d_{d2}\left(\frac{C_{1b}}{C_2}\right)+d_{d3}\left(\frac{C_{1c}}{C_2}\right)\right)V_{REF} \Rightarrow V_{OUTk}=4V_{INk}-\left(d_{dd1}+d_{dd2}+d_{dd3}\right)V_{REF}$$

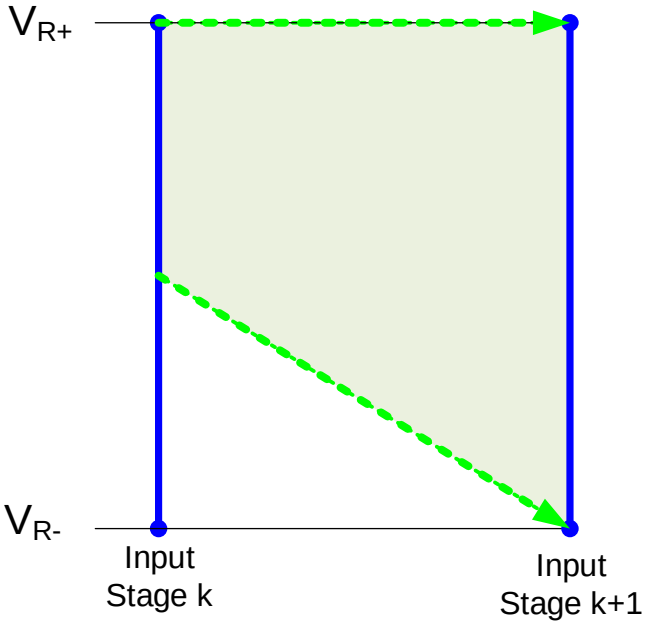
- Use thermometer code outputs
- Can be extended to more bits/stage
- Accurate gain possible with good layout

Operation of Pipelined Amplifier

Ideal transfer characteristics (1 bit/stage)

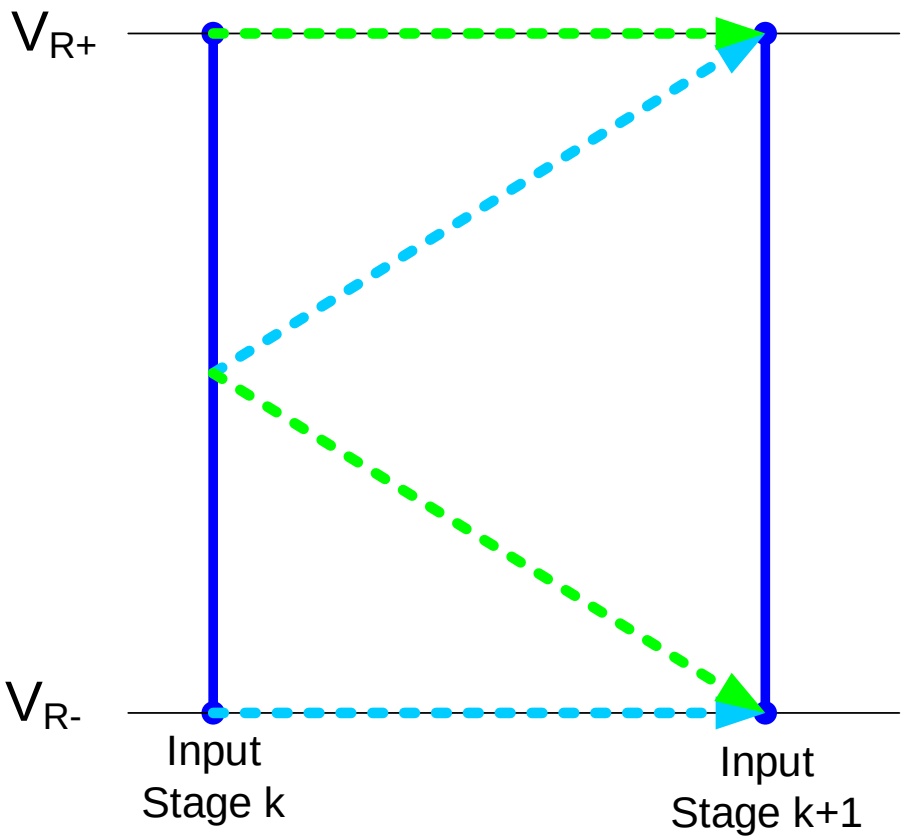


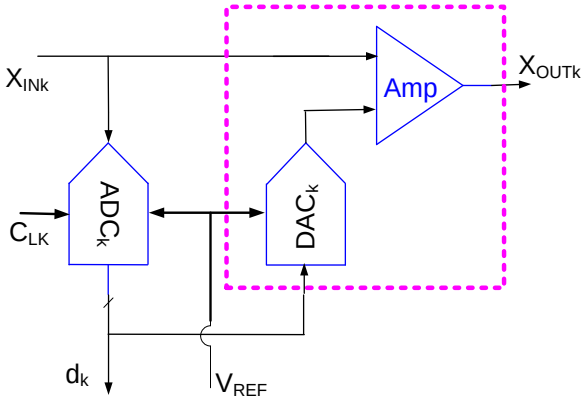




Operation of Pipelined Amplifier

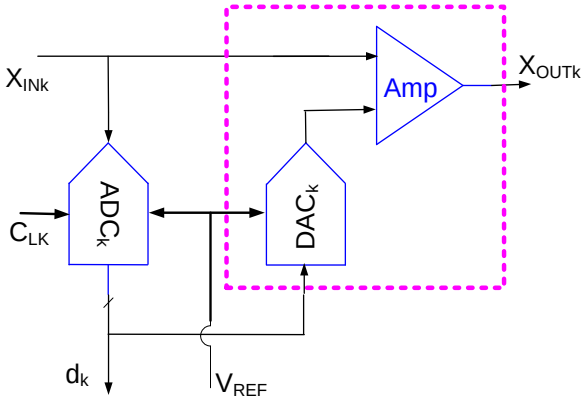
Ideal transfer characteristics (1 bit/stage)

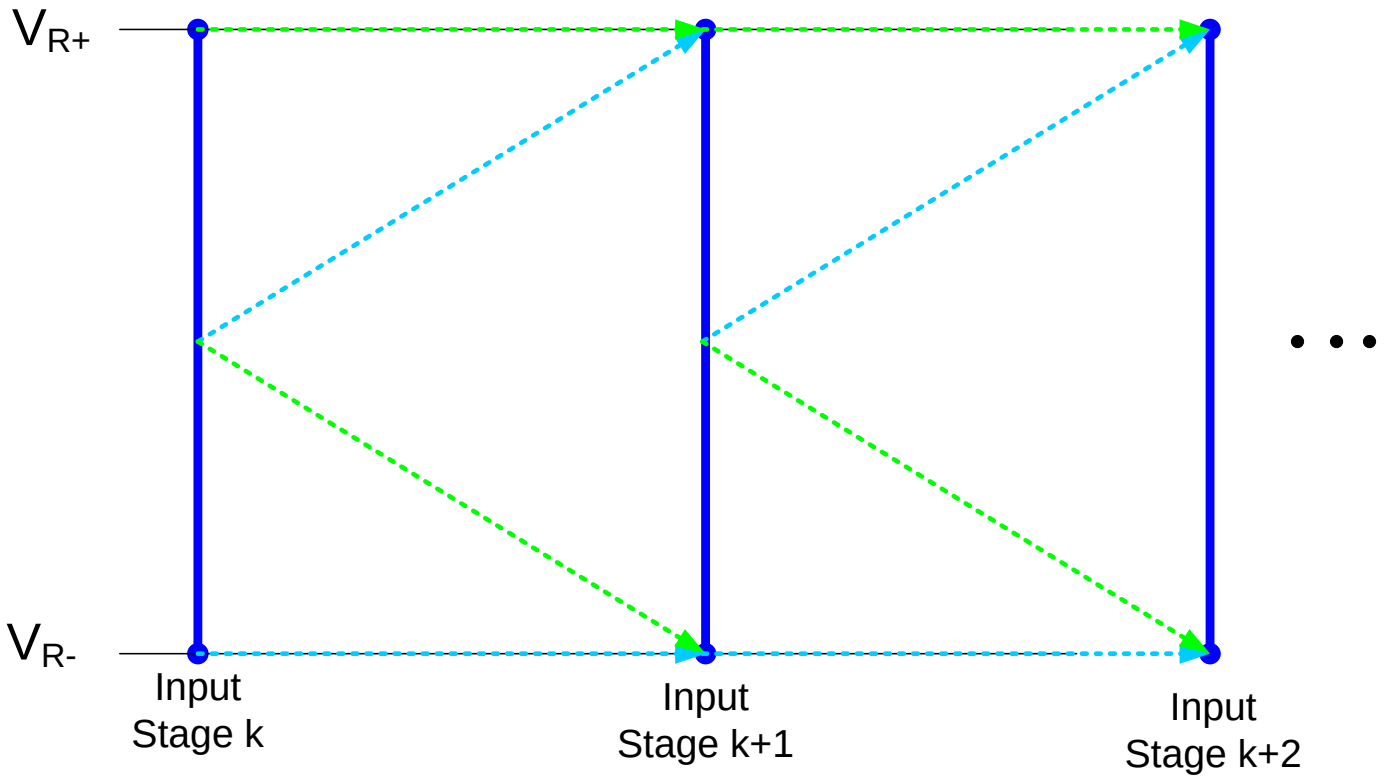




Operation of Pipelined Amplifier

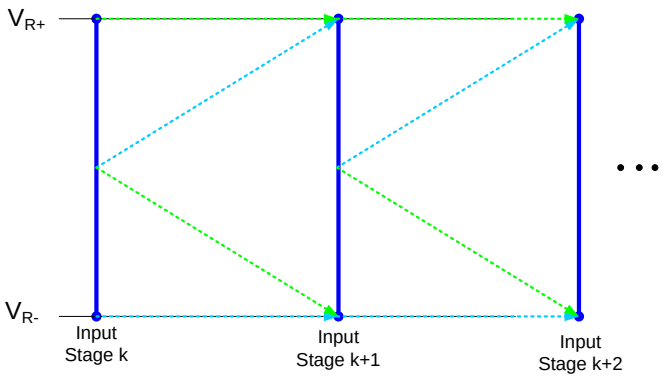
Ideal transfer characteristics (1 bit/stage)

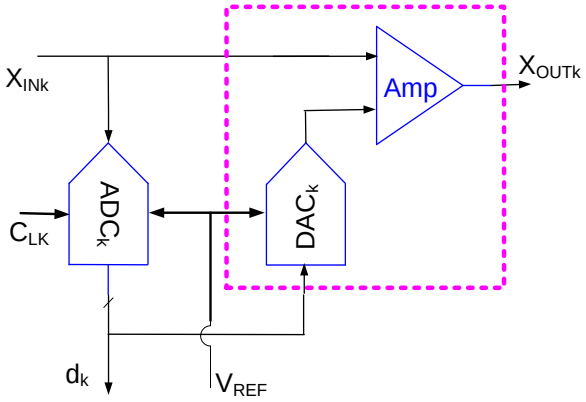


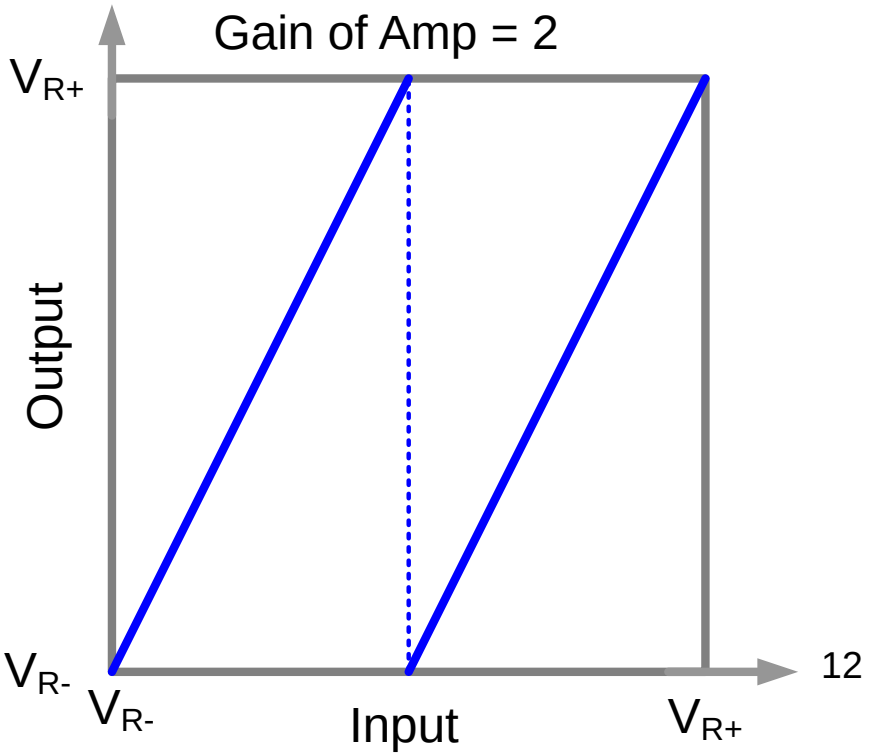


Operation of Pipelined Amplifier

Ideal transfer characteristics (1 bit/stage)

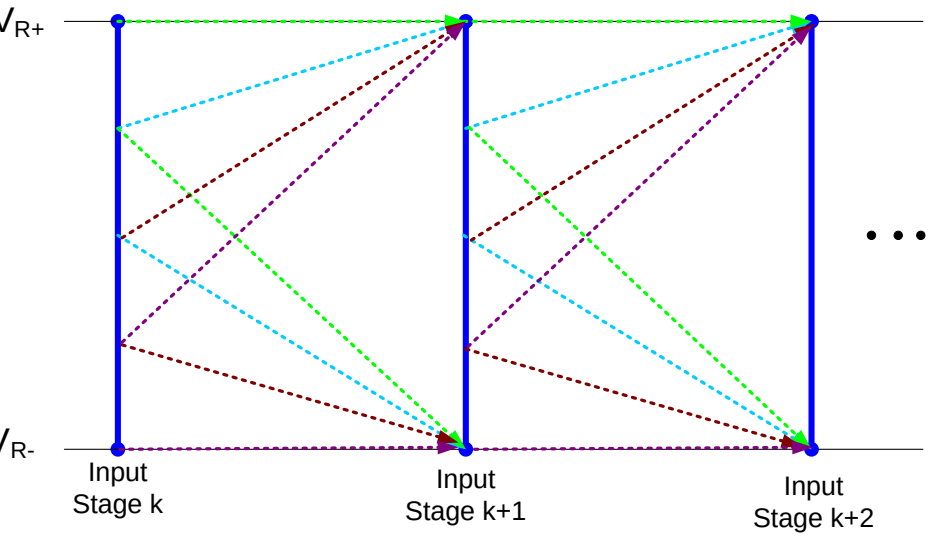


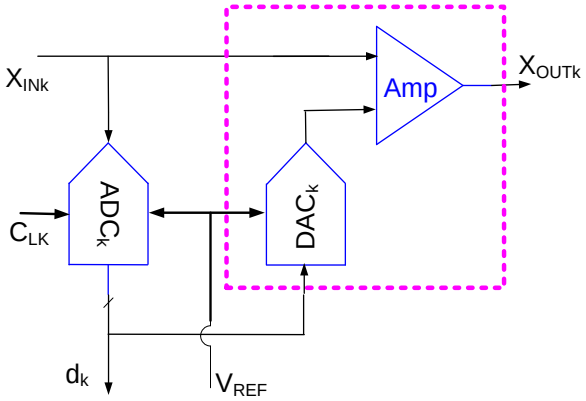


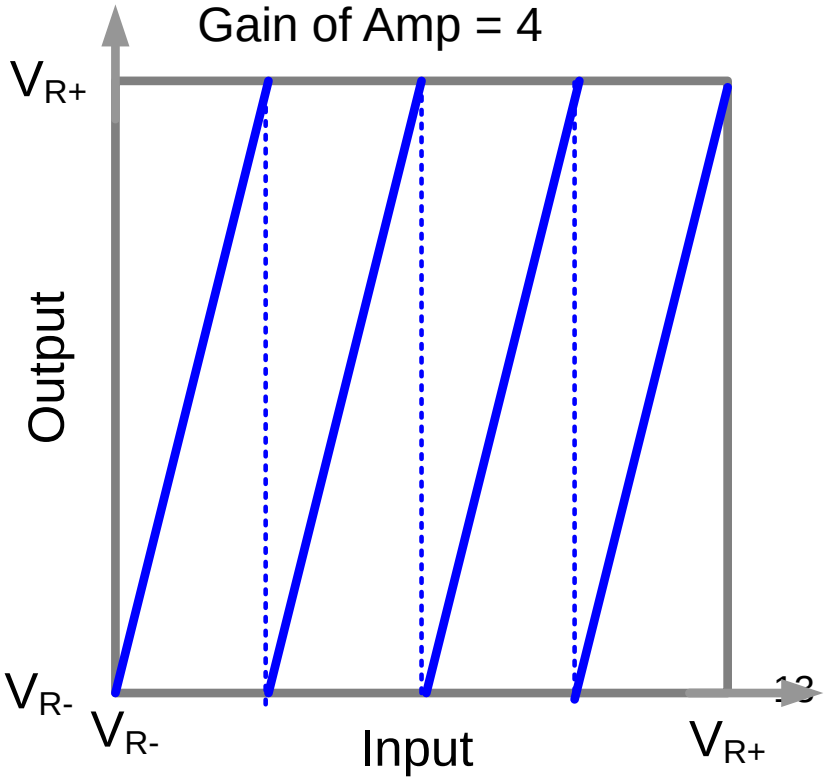


Operation of Pipelined Amplifier

Ideal transfer characteristics (2 bits/stage)

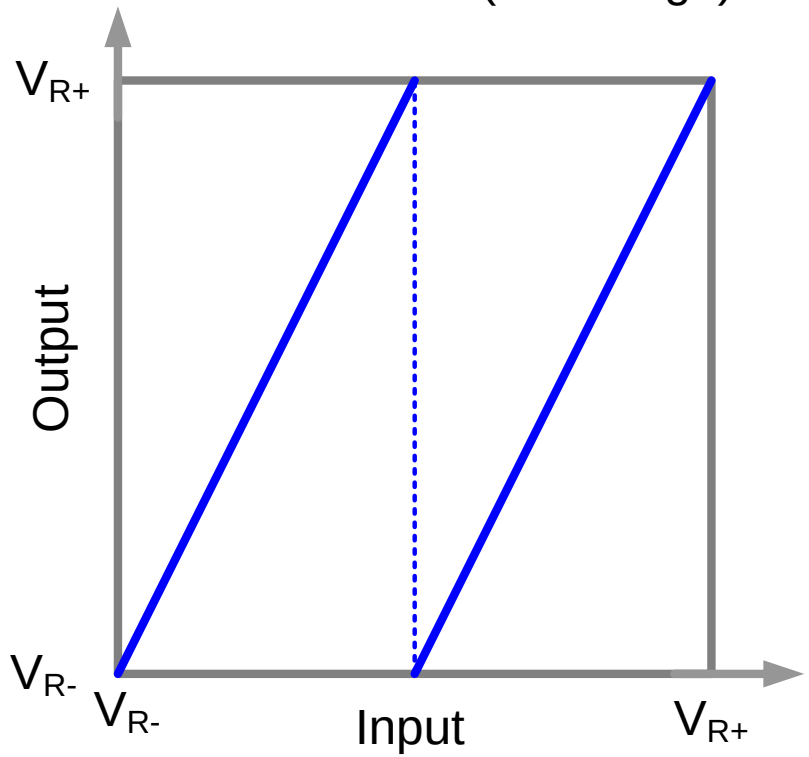


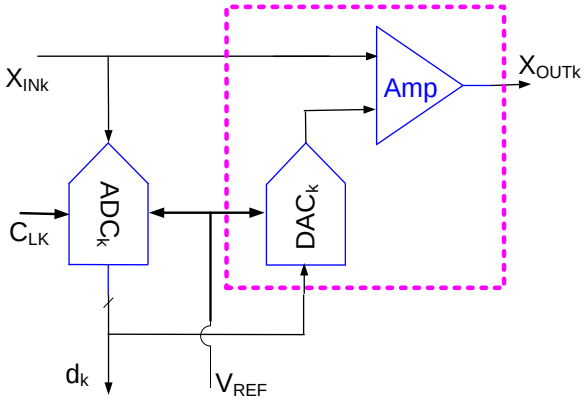




Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

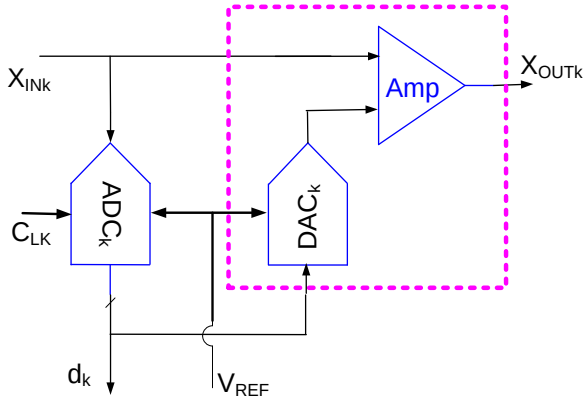




But what really happens?

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



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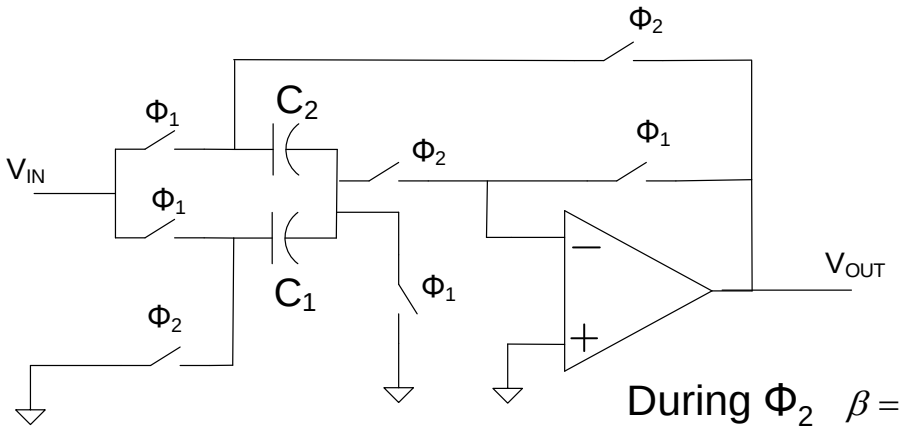
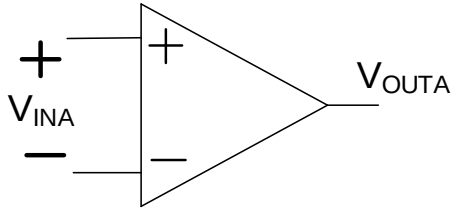
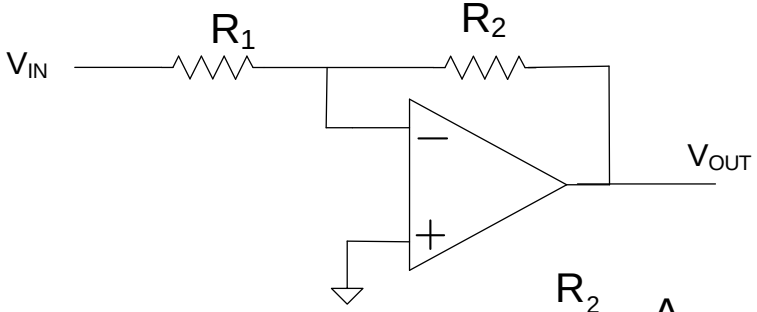


During Φ_2 $\beta = \frac{C_2}{C_1 + C_2}$





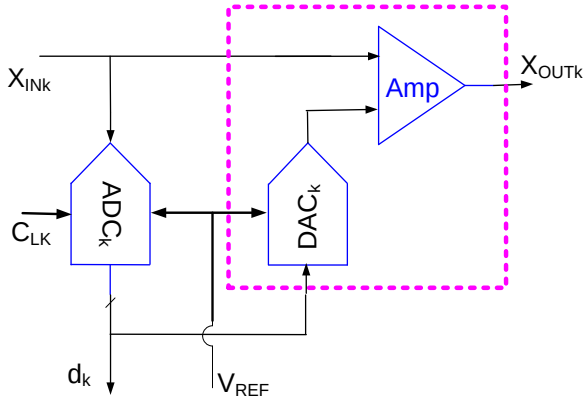
$$\beta = \frac{R_1}{R_1 + R_2}$$

$$A_{FB} = \frac{-\frac{R_2}{R_1 + R_2} A}{1 + A\frac{R_1}{R_1 + R_2}} = \frac{-\theta A}{1 + A\beta} = \frac{-\frac{R_2}{R_1} A\beta}{1 + A\beta}$$

$$A_{FB} = \frac{\theta A}{1 + A\beta} \underset{|A| \neq \infty}{\neq} \frac{\theta}{\beta}$$

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



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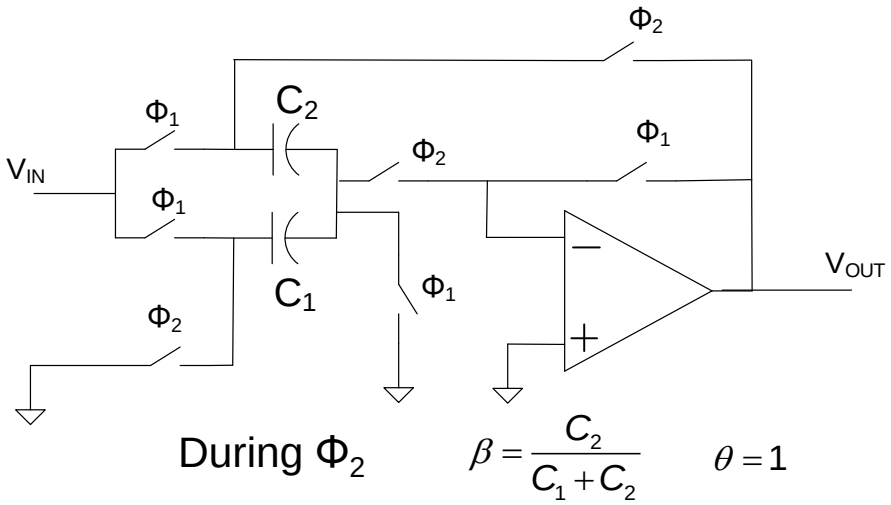


During Φ_2 $\quad \beta = \frac{C_2}{C_1 + C_2}$ $\quad \theta = 1$

$$A_{FB} = \frac{\theta A}{1 + A\beta} \underset{|A| \neq \infty}{\neq} \frac{\theta}{\beta}$$

If ideally C_1=C_2 so that ideal gain is 2, will the actual gain be larger or smaller than 2?

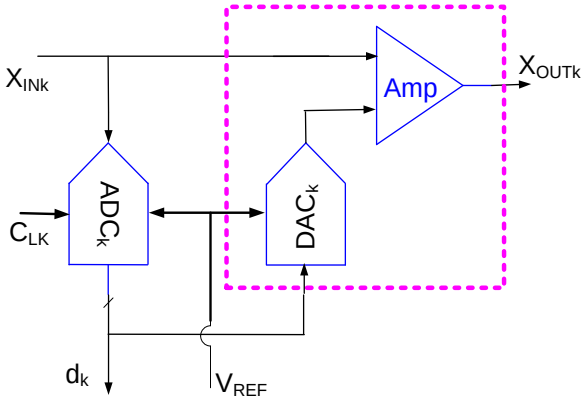
Depends:

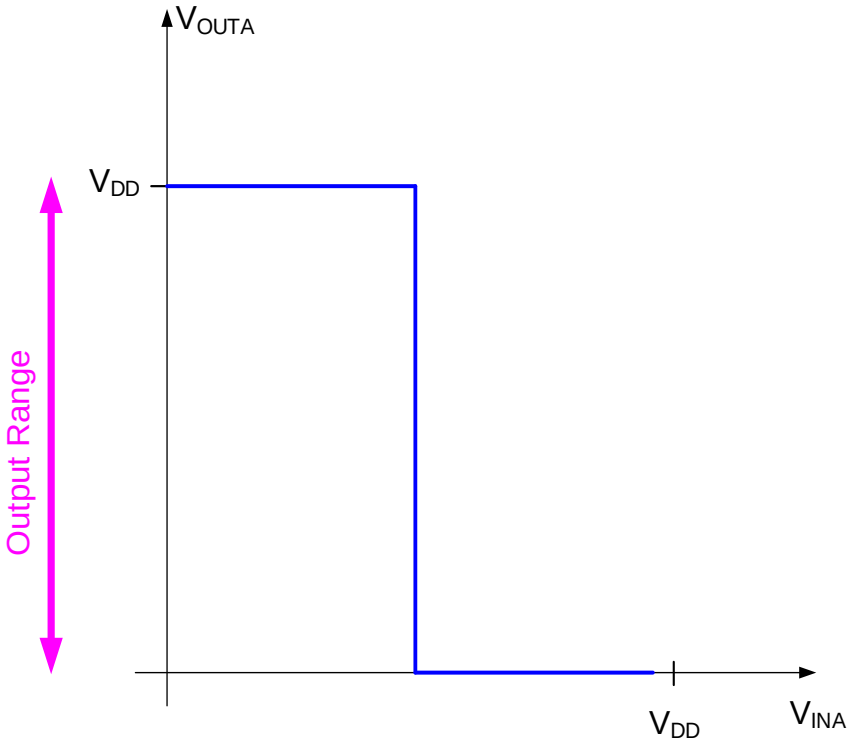
- Finite gain of Op Amp tends to make actual gain < 2
- Capacitor mismatch could make gain larger or smaller than 2
- For reasonable gain in Op Amp, mismatch effects likely will dominate

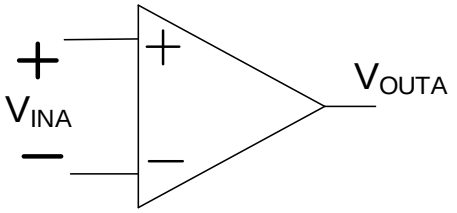
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

But what really happens?





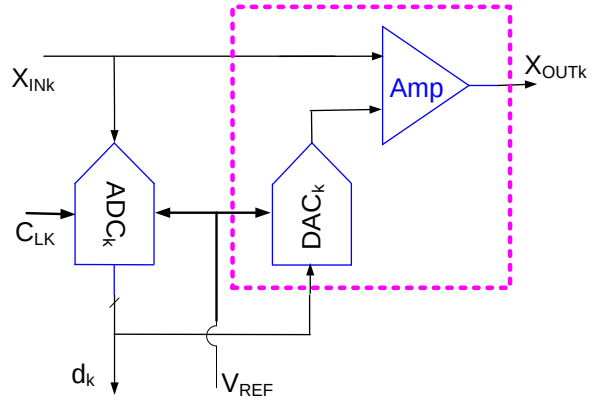


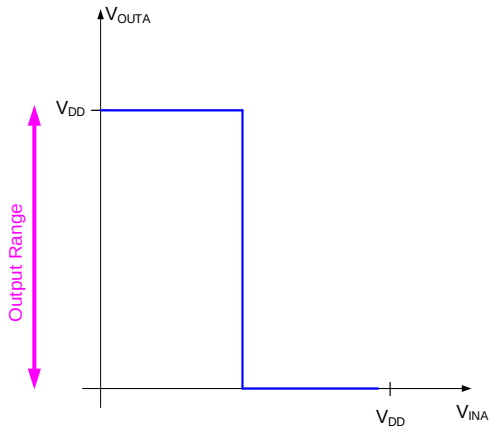
Ideal Op Amp Transfer Characteristics

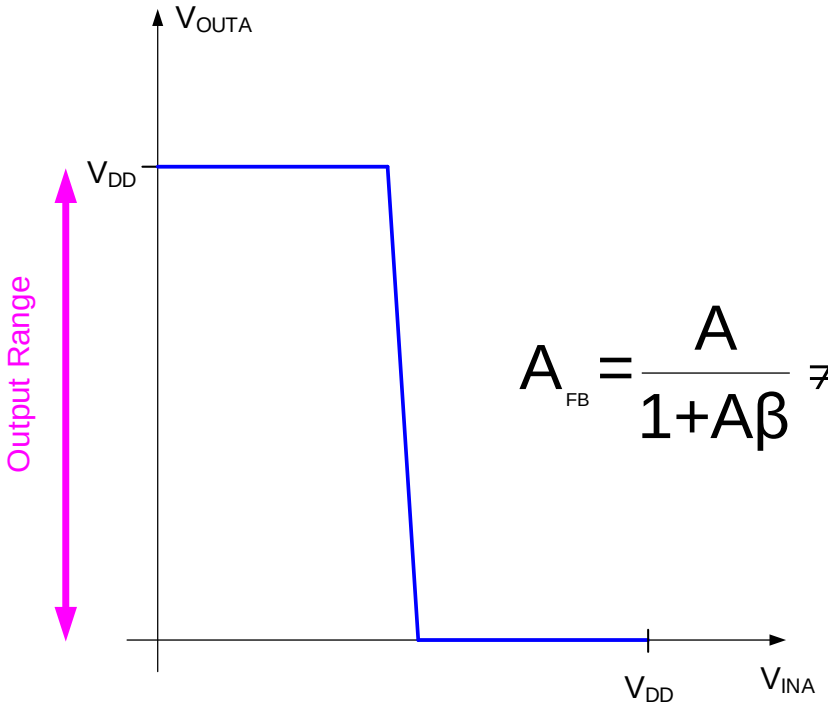
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

But what really happens?





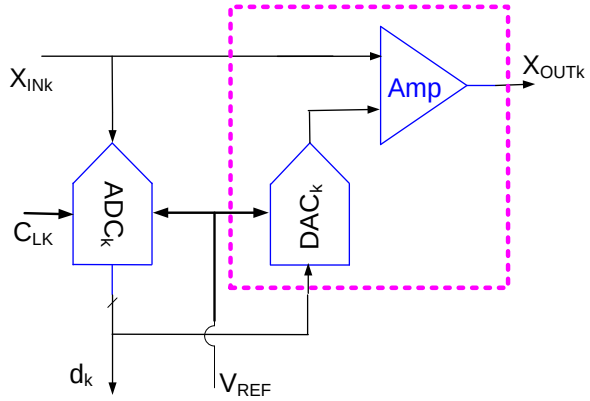


$$A_{FB} = \frac{A}{1+A\beta} \neq \frac{1}{\beta}$$

Finite Op Amp Gain

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



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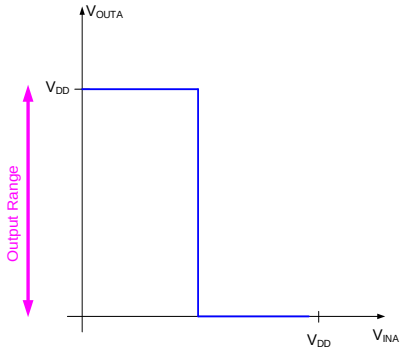
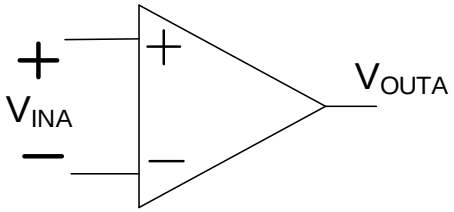
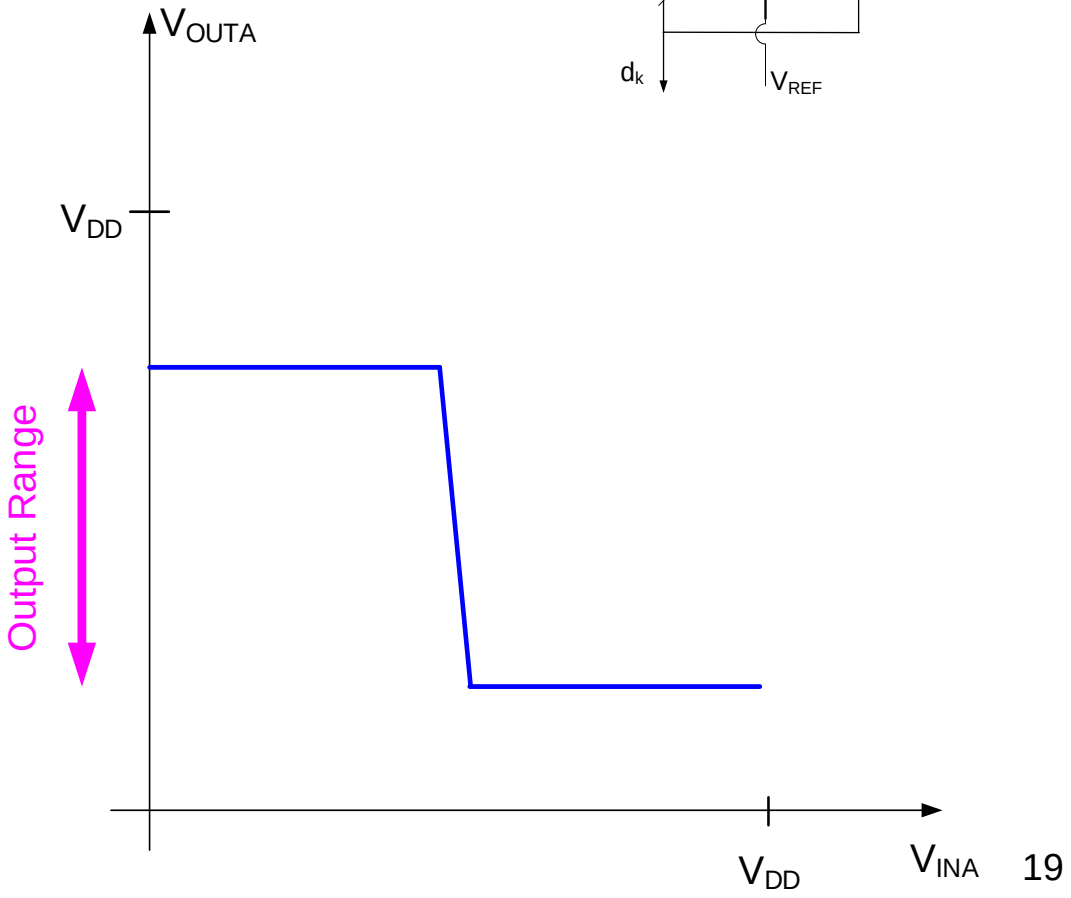




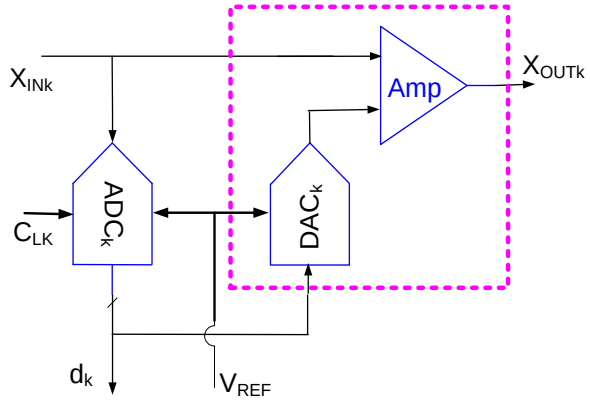


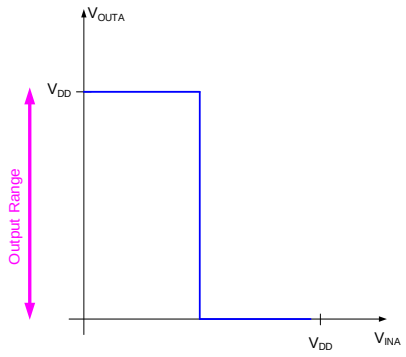
Output Range Limited

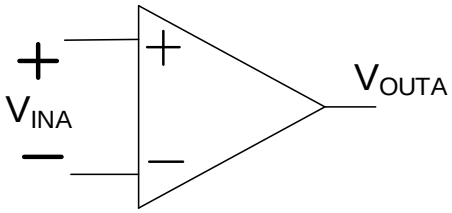
Interstage Amplifiers

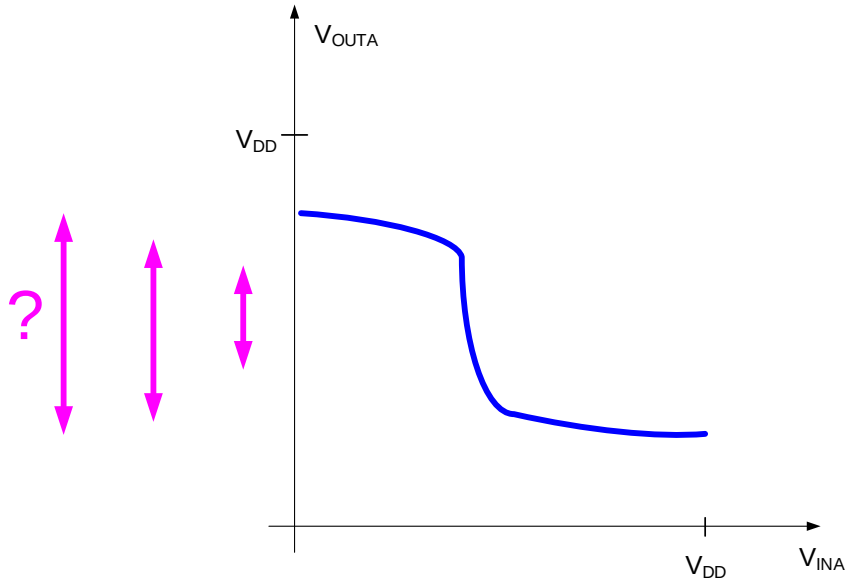
Ideal transfer characteristics (1 bit/stage)

But what really happens?





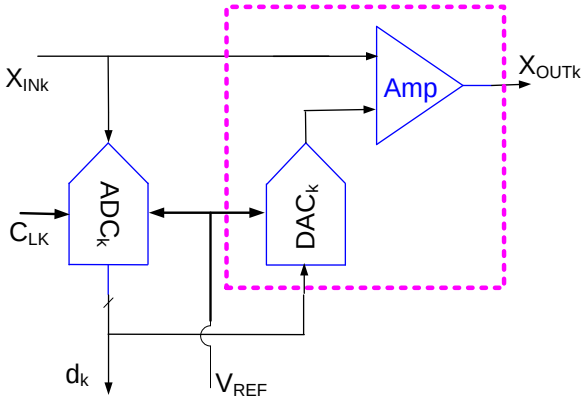




Output Range Limited and Transfer Characteristics are Nonlinear

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



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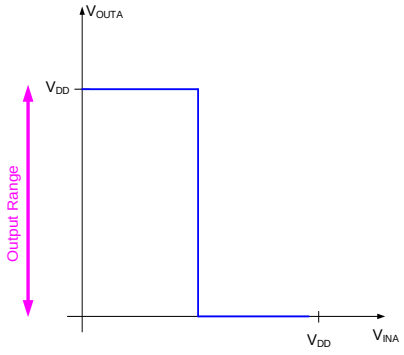
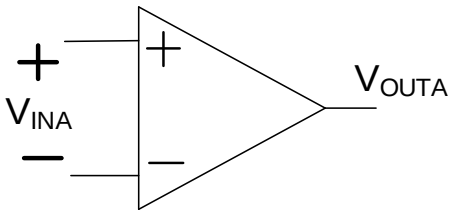
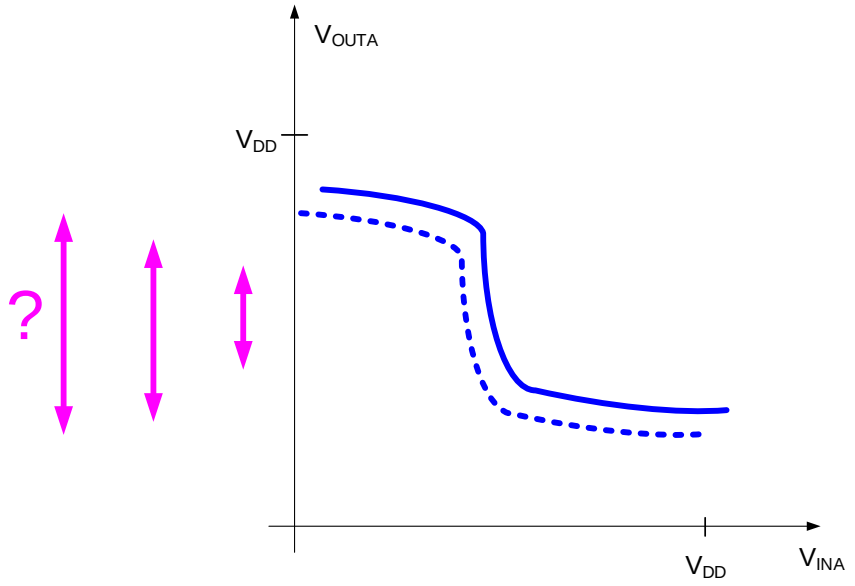




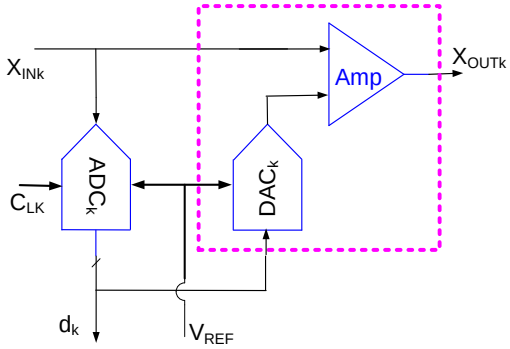


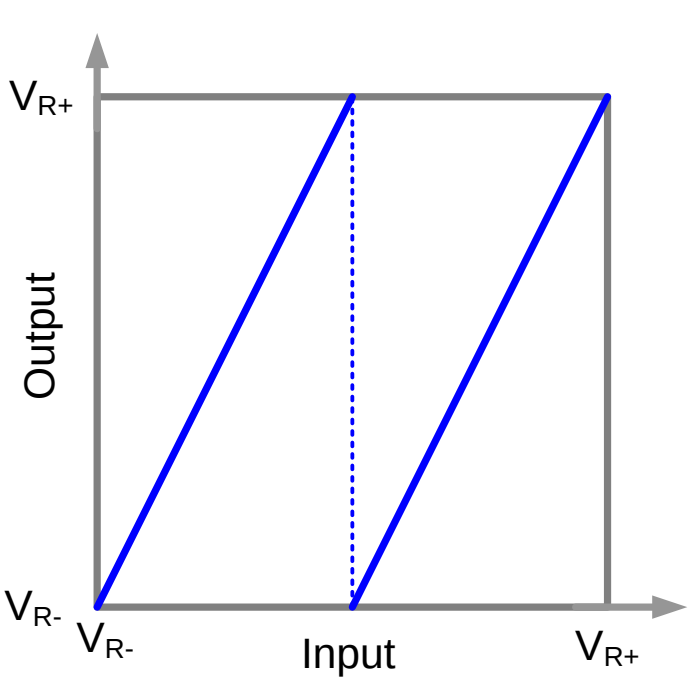
Offsets occur as well

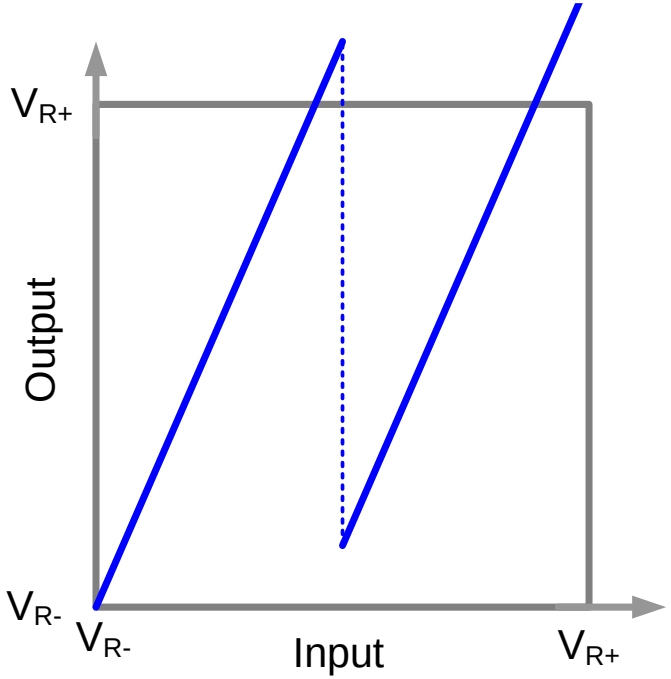
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

What are the effects of these errors?



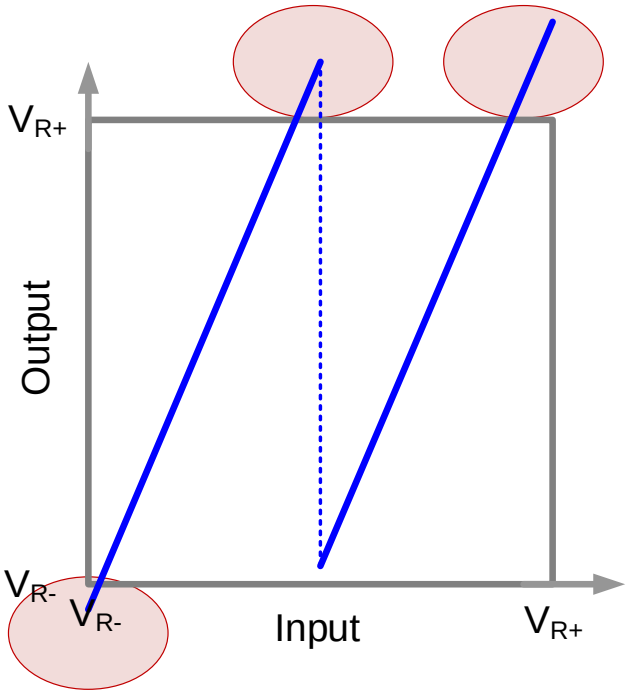


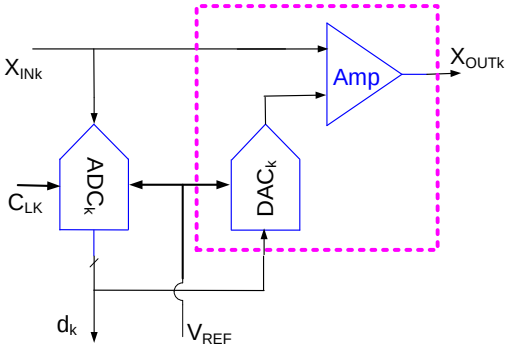


Effect of Gain Error
(for A_{FB}>2)

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



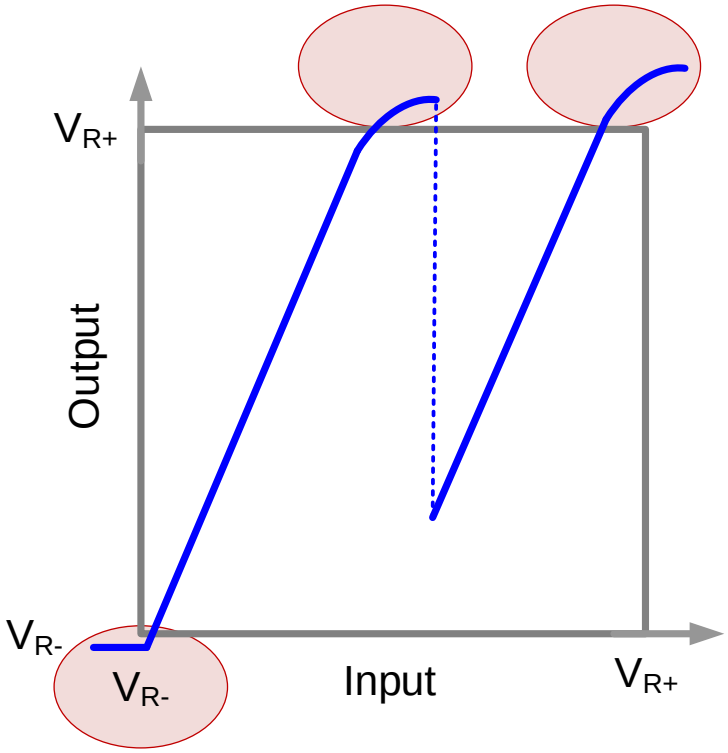


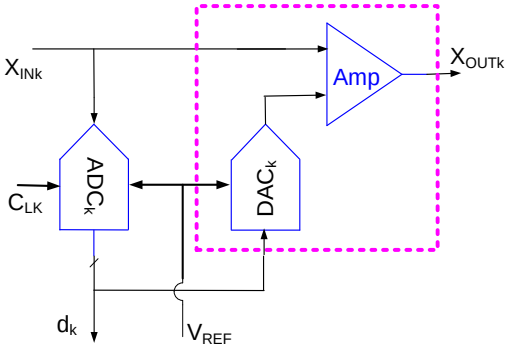
Amplifier/DAC/SH block generally designed to operate well only if residue is internal to the I/O Box

Any place where the output extends beyond the I/O box, data converter is vulnerable to loosing data

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



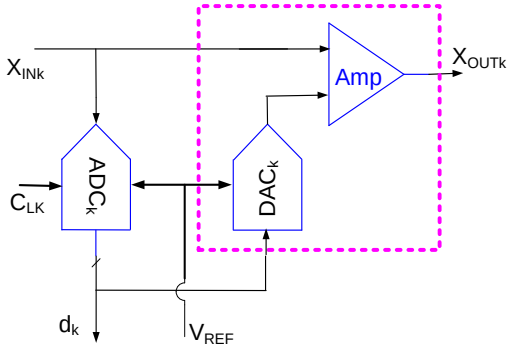


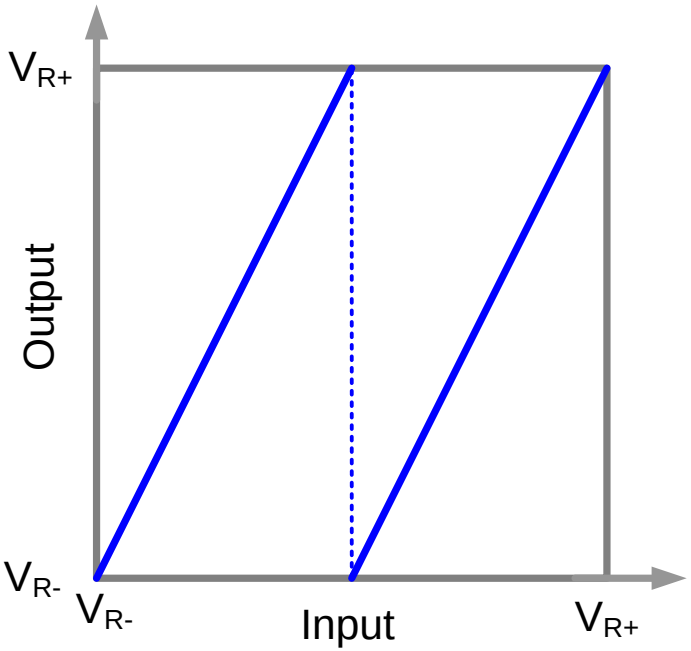
Possible effects of over-range on transfer characteristics of Amplifier/DAC/SH block

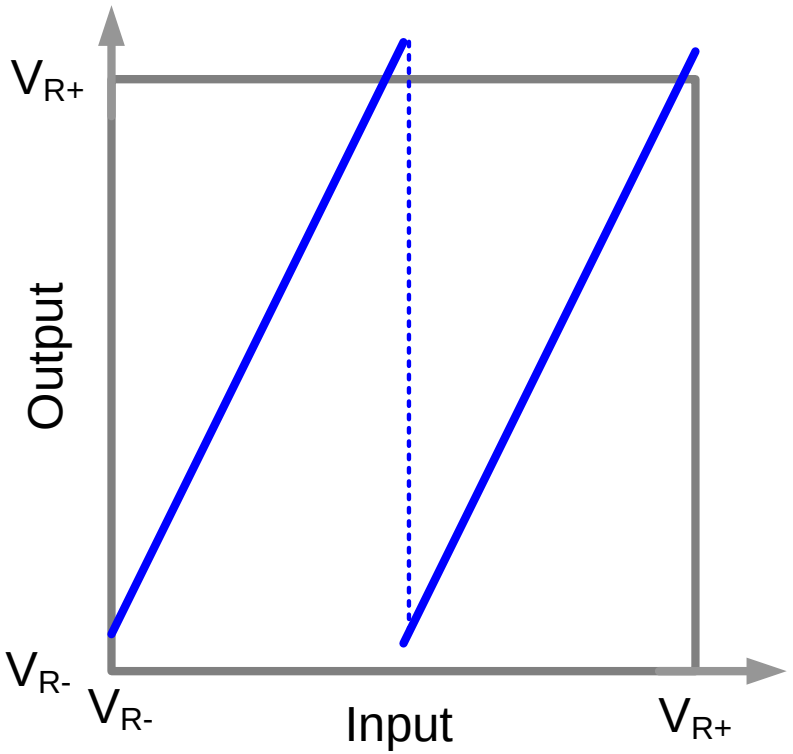
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

What are the effects of these errors?





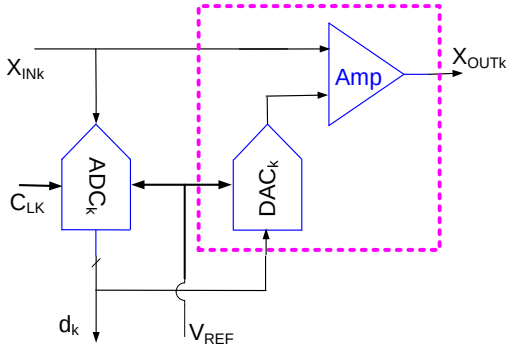


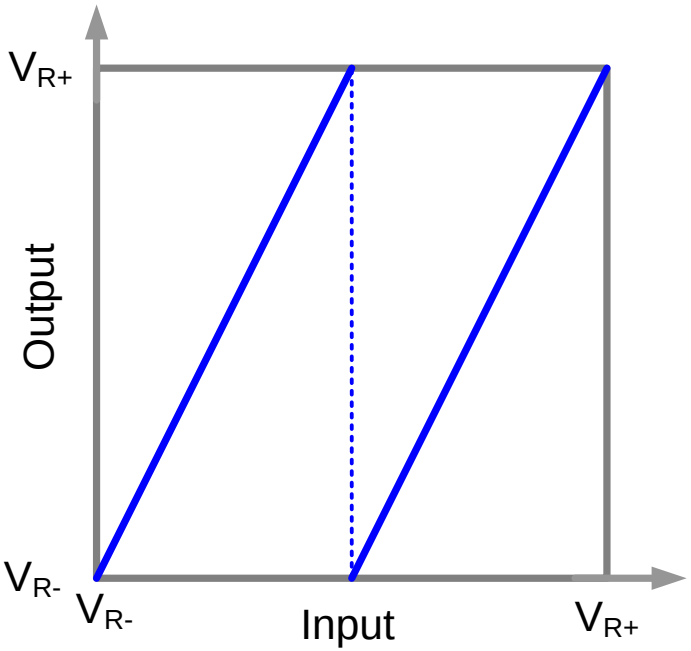
Effect of Amplifier Offset

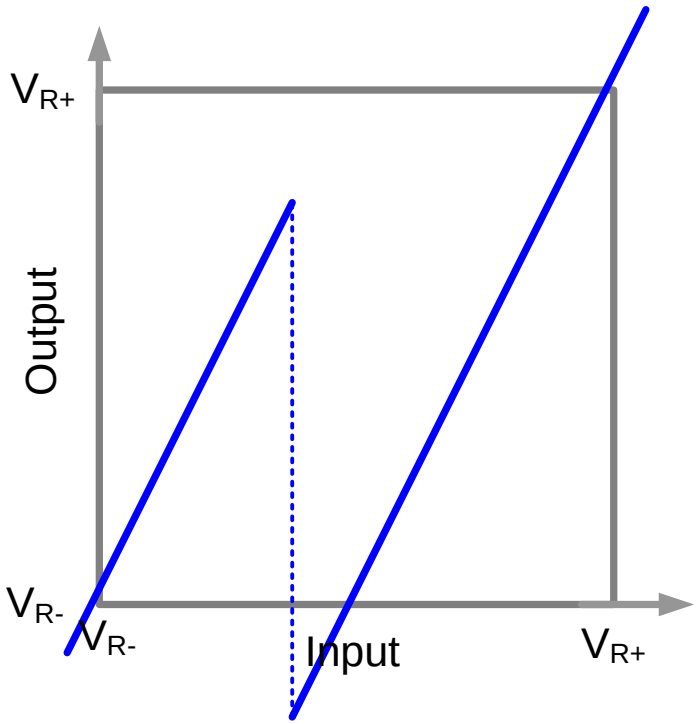
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

What are the effects of these errors?





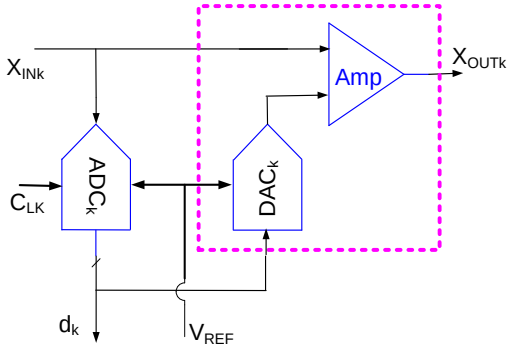


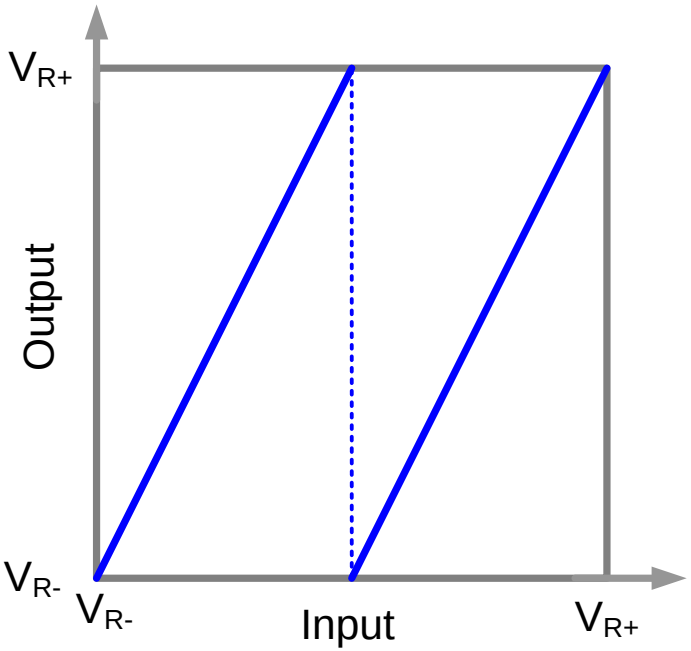
Effect of ADC Offset

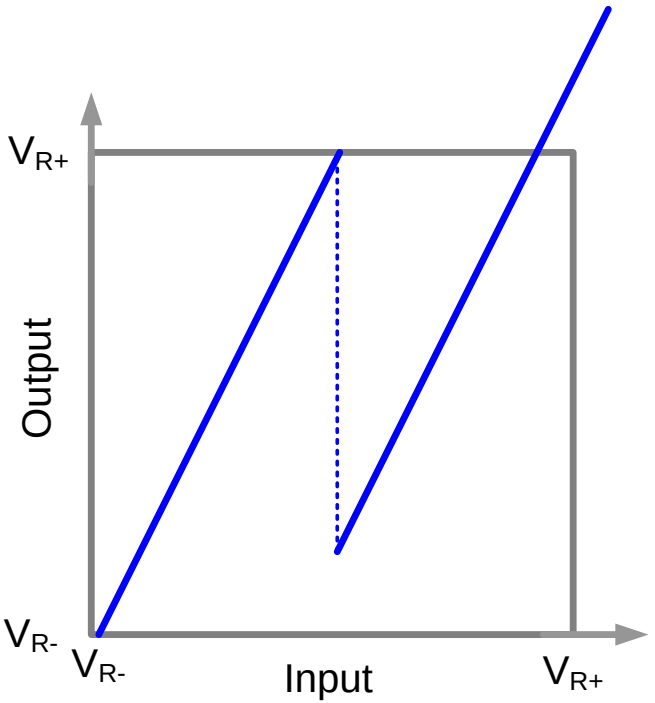
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

What are the effects of these errors?





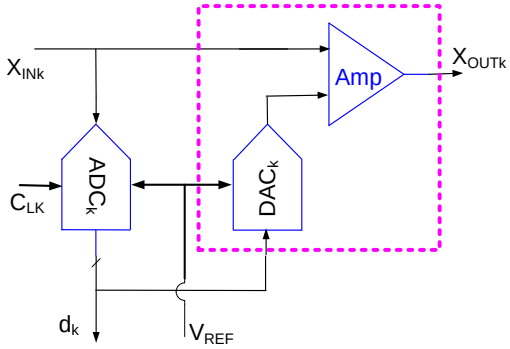


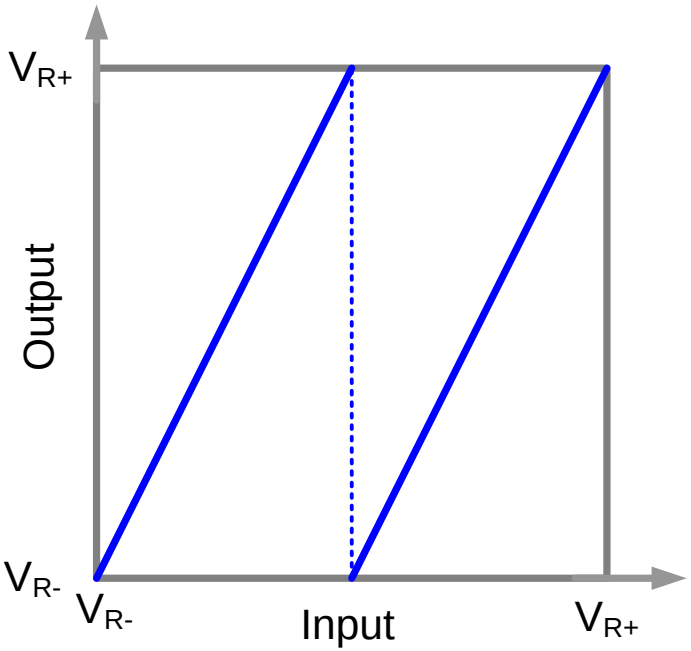
Effect of DAC Errors

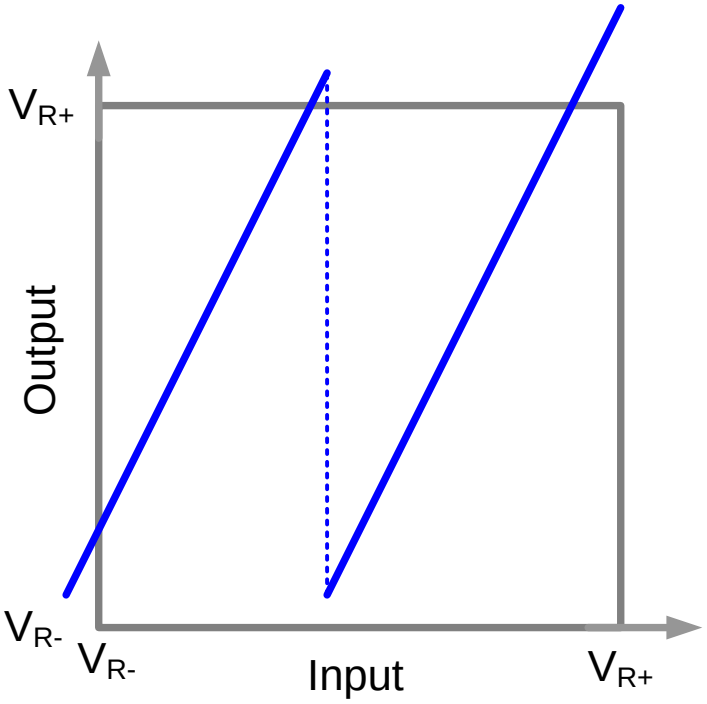
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

What are the effects of these errors?

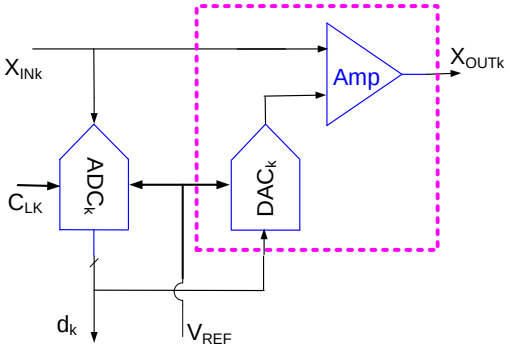






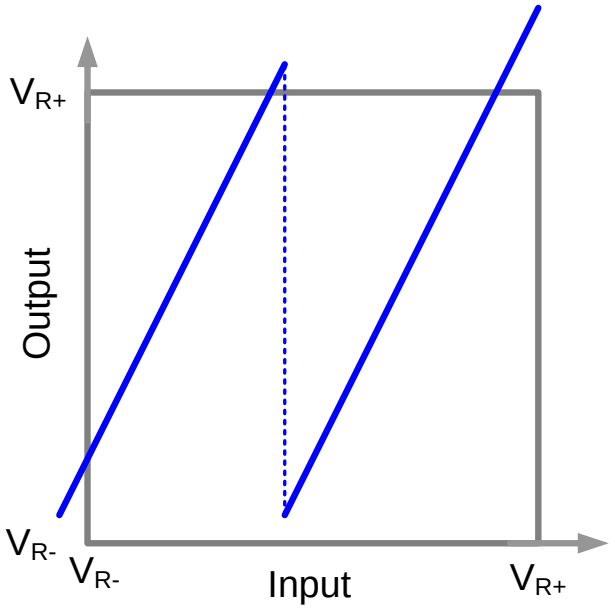
Effects of Simultaneous Errors

Interstage Amplifiers



Ideal transfer characteristics (1 bit/stage)

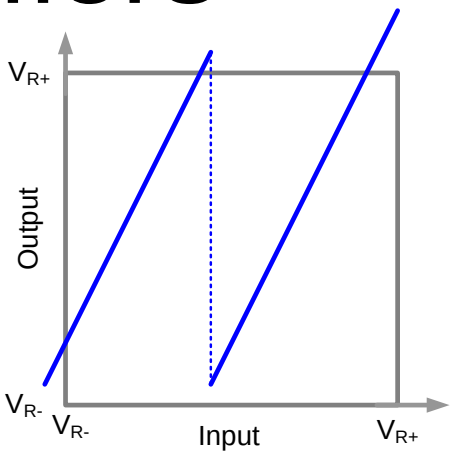
What are the effects of these errors?



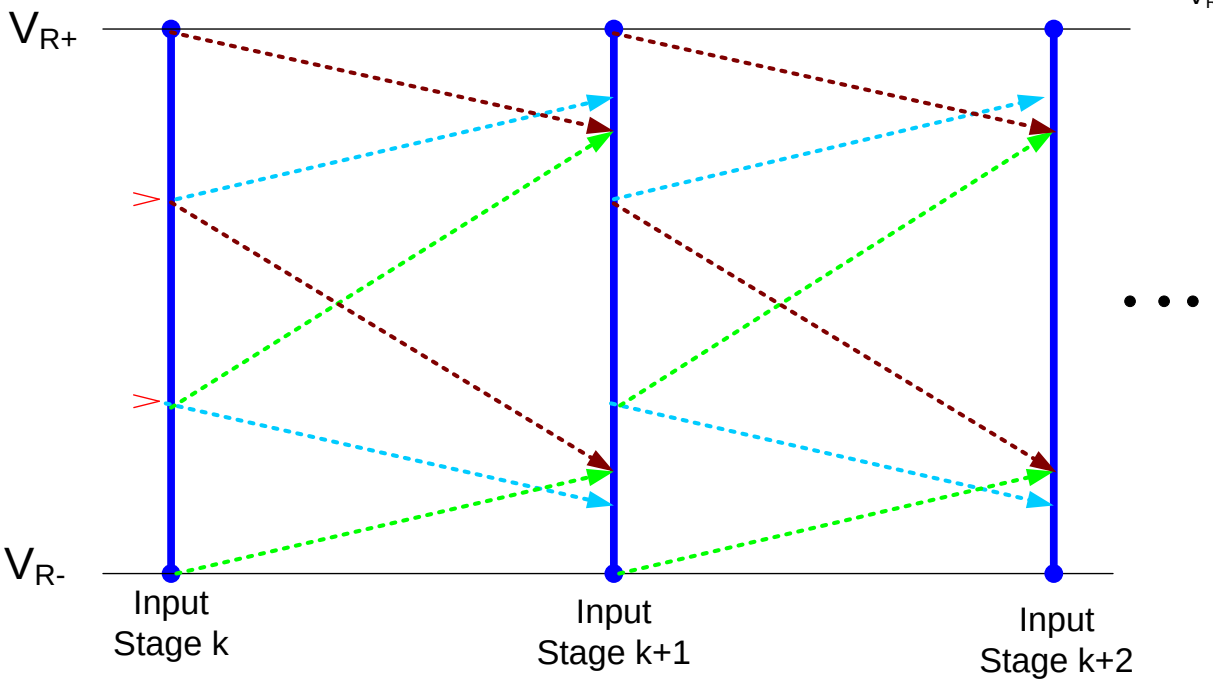
- Incorrect Interpretation of Digital Output Codes
- Over-range of amplifier Inputs (saturating nonlinearities)
- Over-range of Residue at n-1 stage

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



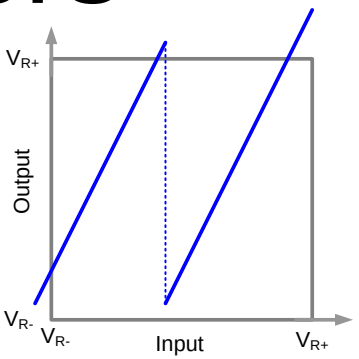
Over-range Protection



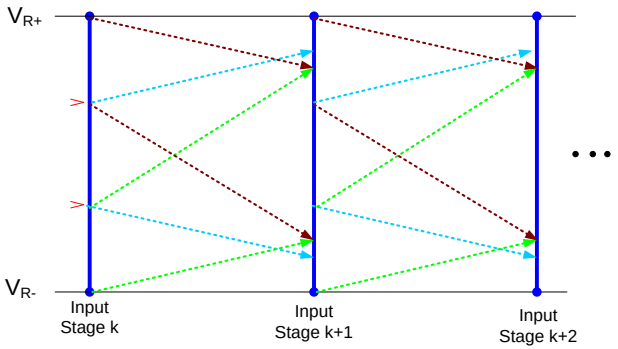
Extra comparator levels in ADC

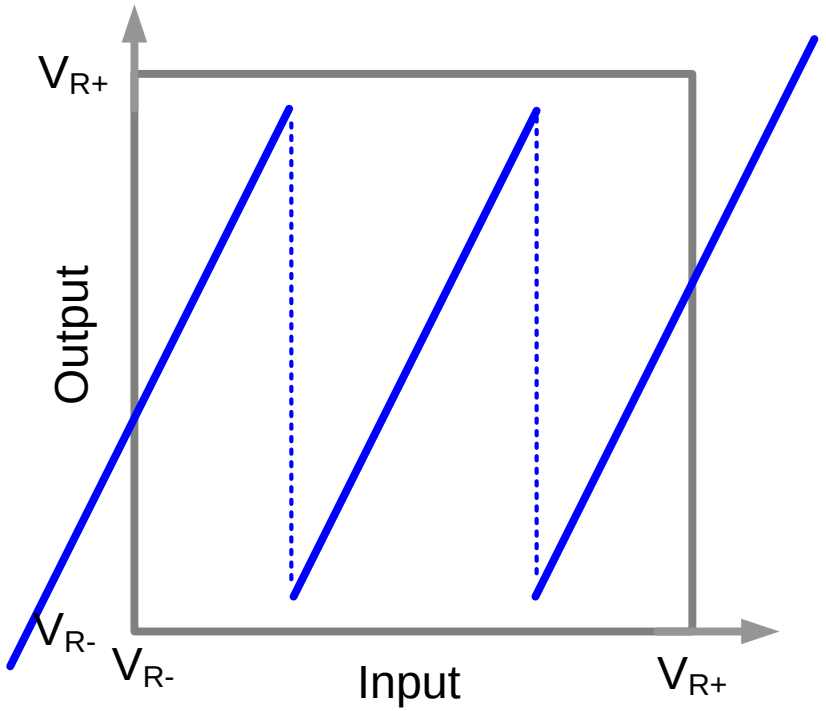
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



Over-range Protection

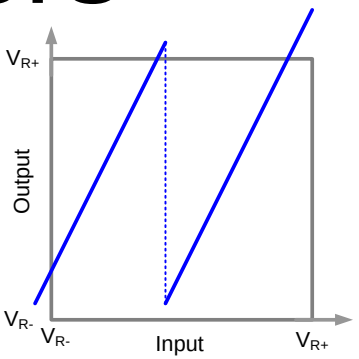




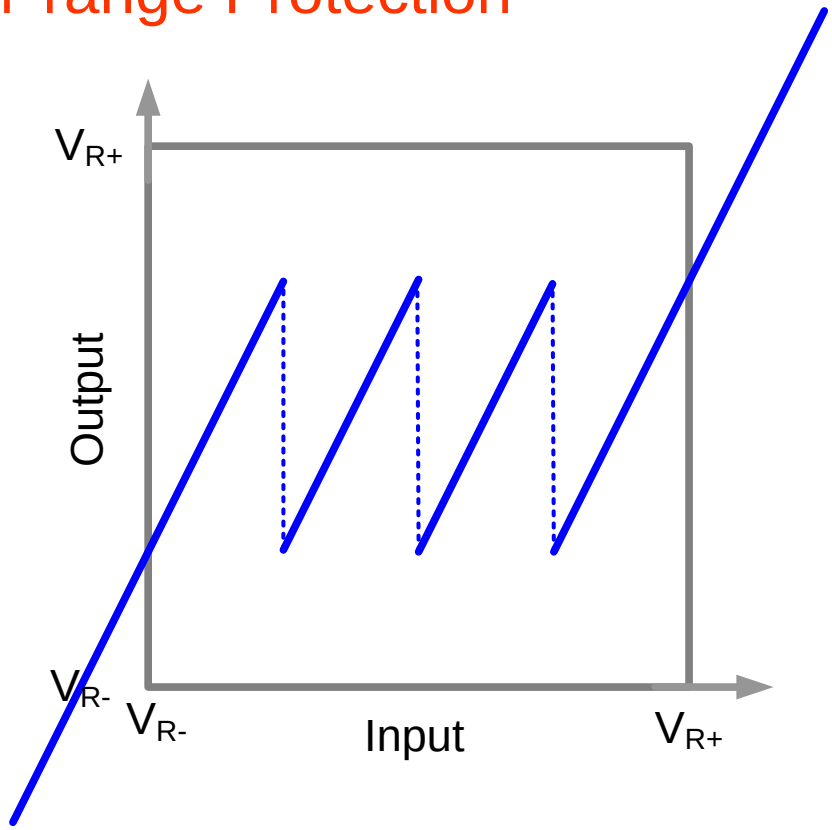
Extra comparator levels in ADC (1 extra comparator)

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



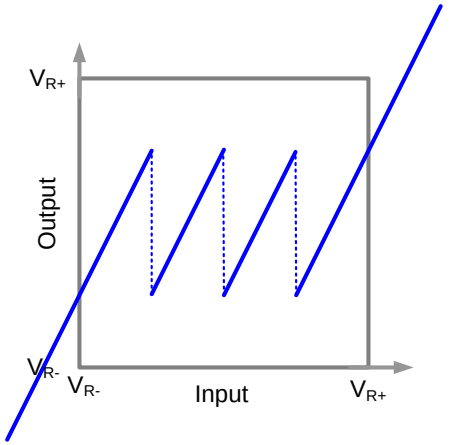
Over-range Protection



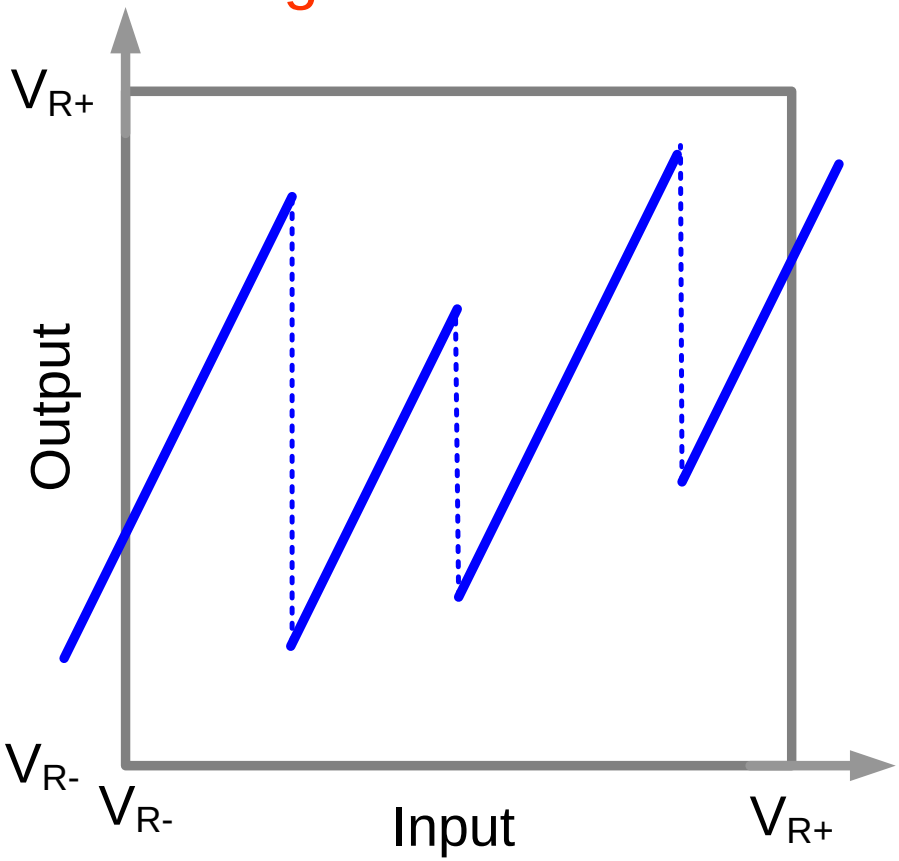
Extra comparator levels in ADC (2 extra comparators)

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



Over-range Protection



Extra comparator levels in ADC (2 extra comparators)

Issues with out-range protection with extra comparators

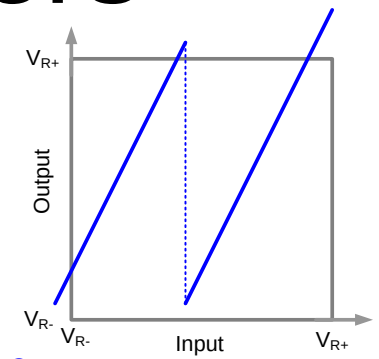
Robust to large levels of comparator offset voltage

Increased dynamic power dissipation and loading of V_{IN} bus

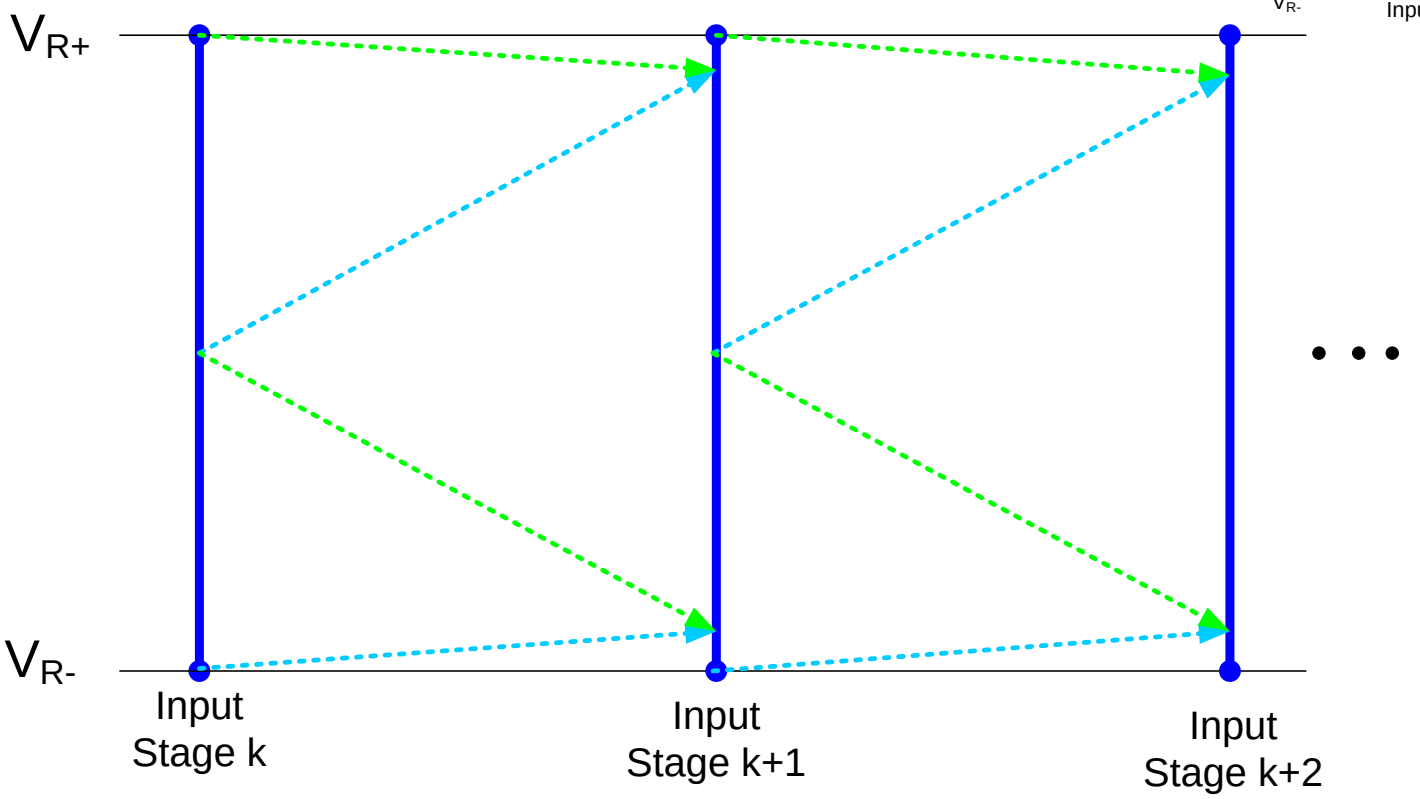
Increase in area

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



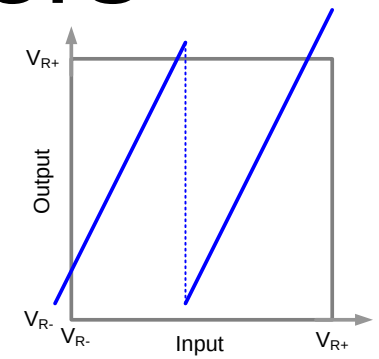
Over-range Protection



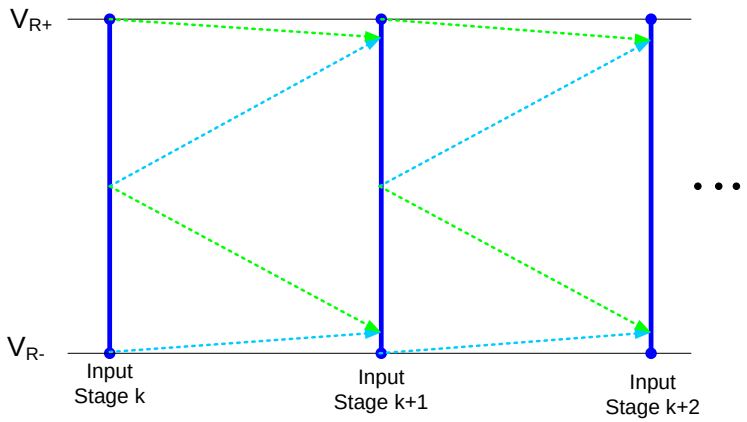
Sub-radix Structure

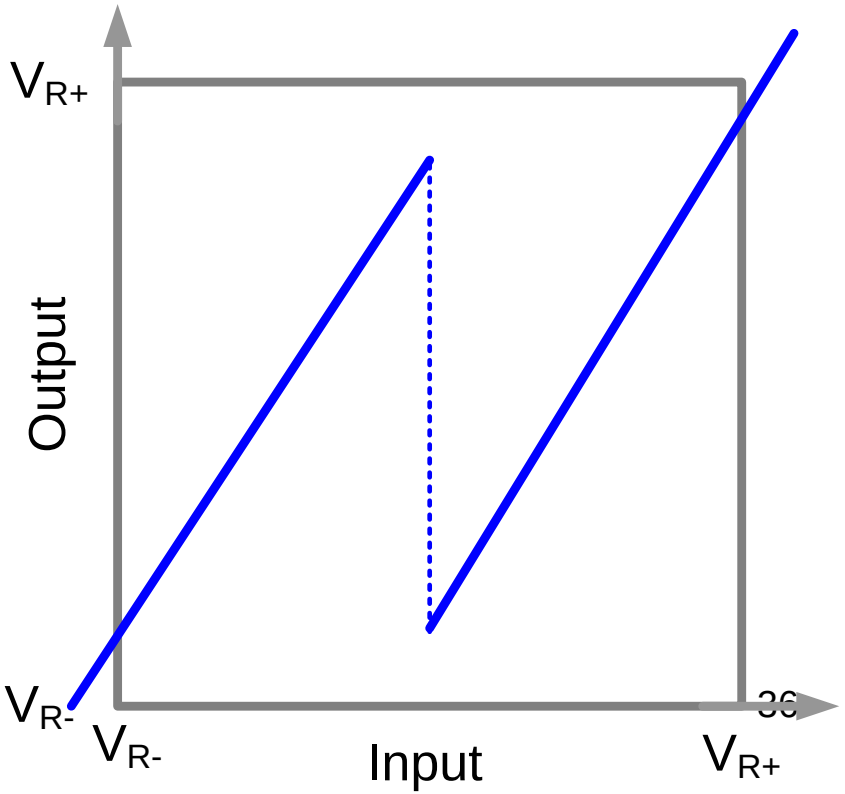
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



Over-range Protection



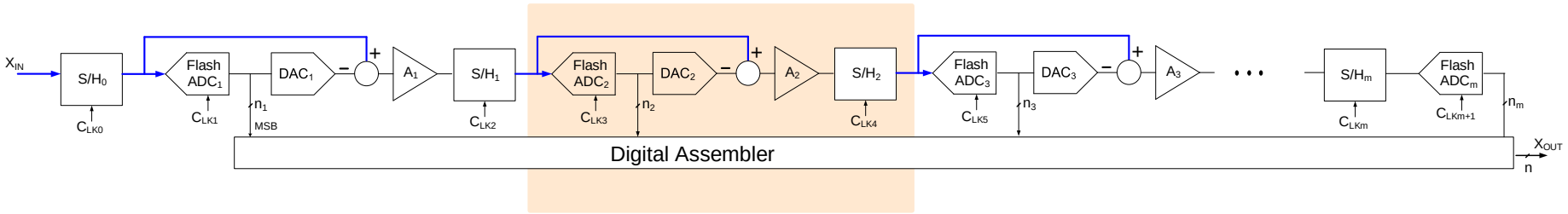


Sub-radix Structure

Issues with sub-radix protection

- Robust to large levels of comparator offset voltage
- Requires more involved adders when output code is re-assembled
- Requires additional stages in pipeline (but at LSB end so power and matching requirements are relaxed

Pipelined ADC



Claim: If the Amplifiers are linear, settling is complete, and over-range protection is provided, the pipelined ADC makes no errors if the output of the DACs are correctly interpreted

Implication: Flash ADC errors, offsets in comparators and amplifiers, and gain errors in amplifier and S/H do not degrade performance of a pipelined ADC structure !!

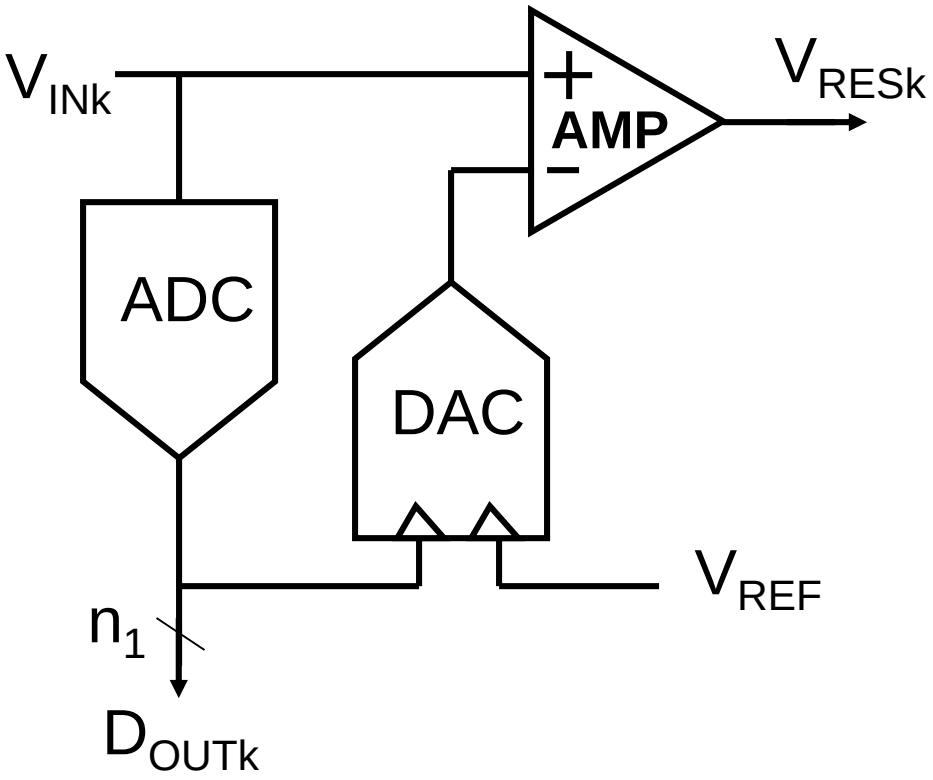
Modeling of a Pipelined ADC

Assumptions:

- All nonlinearities can be neglected
- Settling of Amplifies and DACs is complete
- Over-range protection is provided

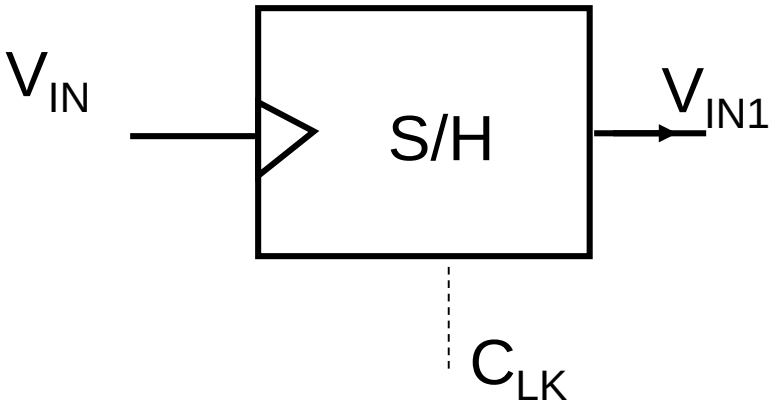
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

- Parameterization of Stage k
  - Amplifier
    - Closed-Loop Gain
      - From input – m_{1k}
      - From DAC – m_{2k}
      - From offset – m_{3k}
    - Offset Voltage - V_{OSk}
  - DAC
    - V_{DACki}
  - ADC
    - Offset Voltages - V_{OSAki}
  - Out-Range Circuit (if used and not included in ADC/DAC)
    - DAC Levels - V_{DACBki}
    - Amplifier Gain – m_{4k}



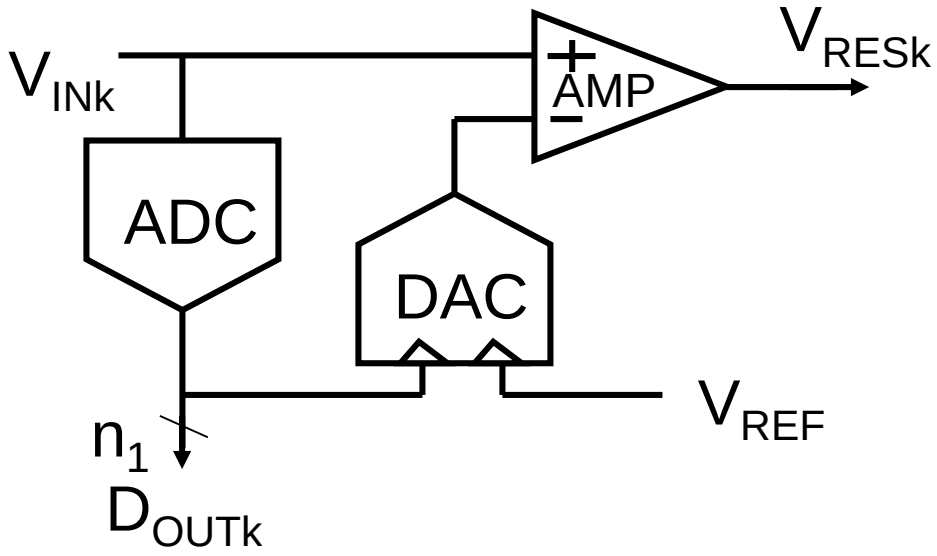
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC

- **Parameterization of Input S/H Stage**



$$V_{in1} = m_{10} V_{in} + m_{20} V_{OS0}$$

Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC



For notational convenience, assume 1 bit/stage

$$V_{RESk} = m_{1k} V_{ink} - d_k V_{DACk} m_{2k} + m_{3k} V_{OSk}$$

with 1 bit/stage, $V_{DACk}=V_{REF}/2$ for all k

Mathematical Representation of the n Pipelined Stages

$$V_{RES1} = m_{11} V_{in1} - d_1 V_{DAC1} m_{21} + m_{31} V_{OS1}$$

$$V_{RES2} = m_{12} V_{in2} - d_2 V_{DAC2} m_{22} + m_{32} V_{OS2}$$

$$\bullet \bullet \bullet$$

$$V_{RESk} = m_{1k} V_{ink} - d_k V_{DACk} m_{2k} + m_{3k} V_{OSk}$$

$$\bullet \bullet \bullet$$

$$V_{RES(n-1)} = m_{1(n-1)} V_{in(n-1)} - d_{(n-1)} V_{DAC(n-1)} m_{2(n-1)} + m_{3(n-1)} V_{OS(n-1)}$$

Assume for convenience there is also a residue at the last stage

$$V_{RESn} = m_{1n} V_{inn} - d_n V_{DACn} m_{2n} + m_{3n} V_{OSn}$$

Mathematical Representation of the Pipelined ADC

$$V_{in1} = m_{10} V_{in} + m_{20} V_{OS0}$$

$$V_{RES1} = m_{11} V_{in1} - d_1 V_{DAC1} m_{21} + m_{31} V_{OS1}$$

$$V_{RES2} = m_{12} V_{in2} - d_2 V_{DAC2} m_{22} + m_{32} V_{OS2}$$

$$\bullet \bullet \bullet$$

$$V_{RESk} = m_{1k} V_{ink} - d_k V_{DACk} m_{2k} + m_{3k} V_{OSk}$$

$$\bullet \bullet \bullet$$

$$V_{RES(n-1)} = m_{1(n-1)} V_{in(n-1)} - d_{(n-1)} V_{DAC(n-1)} m_{2(n-1)} + m_{3(n-1)} V_{OS(n-1)}$$

$$V_{RESn} = m_{1n} V_{inn} - d_n V_{DACn} m_{2n} + m_{3n} V_{OSn}$$

Mathematical Representation of the Pseudo-Static Pipelined ADC

$$V_{in1} = m_{10} V_{in} + m_{20} V_{OS0}$$

$$V_{RES1} = m_{11} V_{in1} - d_1 V_{DAC1} m_{21} + m_{31} V_{OS1}$$

$$V_{RES2} = m_{12} V_{in2} - d_2 V_{DAC2} m_{22} + m_{32} V_{OS2}$$

$$\cdots$$

$$V_{RESk} = m_{1k} V_{ink} - d_k V_{DACk} m_{2k} + m_{3k} V_{OSk}$$

$$\cdots$$

$$V_{RES(n-1)} = m_{1(n-1)} V_{in(n-1)} - d_{(n-1)} V_{DAC(n-1)} m_{2(n-1)} + m_{3(n-1)} V_{OS(n-1)}$$

$$V_{RESn} = m_{1n} V_{inn} - d_n V_{DACn} m_{2n} + m_{3n} V_{OSn}$$

$$V_{RESk} = V_{in(k+1)} \qquad \textit{for} \qquad k = 1 \ldots n\text{-}1$$

2n equations relating 2n-1 intermediate nodal voltages and V_{in}

2n unknowns: $\{V_{in1}, V_{in2}, \ldots V_{inn}, V_{RES1}, V_{RES2}, \ldots V_{RESn-1}, V_{in}\}$

Want to solve 2n equations for 2n unknowns to obtain V_{in}

Mathematical Representation of the Pseudo-Static Pipelined ADC

Eliminating V_{RES} terms

$$V_{in1} = m_{10} V_{in} + m_{20} V_{OS0}$$

$$V_{in2} = m_{11} V_{in1} - d_1 V_{DAC1} m_{21} + m_{31} V_{OS1}$$

$$V_{in3} = m_{12} V_{in2} - d_2 V_{DAC2} m_{22} + m_{32} V_{OS2}$$

$$\bullet \bullet \bullet$$

$$V_{in(k+1)} = m_{1k} V_{ink} - d_k V_{DACk} m_{2k} + m_{3k} V_{OSk}$$

$$\bullet \bullet \bullet$$

$$V_{in\_n} = m_{1(n-1)} V_{in(n-1)} - d_{(n-1)} V_{DAC(n-1)} m_{2(n-1)} + m_{3(n-1)} V_{OS(n-1)}$$

$$V_{RESn} = m_{1n} V_{inn} - d_n V_{DACn} m_{2n} + m_{3n} V_{OSn}$$

n equations relating n intermediate nodal voltages and V_{in}

n+1 unknowns: $\{V_{in1}, V_{in2}, \ldots V_{inn}, V_{in}\}$

Want to solve n equations for n+1 unknowns to obtain V_{in}

Appears to **be** over-constrained !

Mathematical Representation of the Pseudo-Static Pipelined ADC

Actually, these equations are nested so a solution may proceed by back substitution (ignoring the over-constrained concern)

$$V_{in1} = m_{10} V_{in} + m_{20} V_{OS0}$$

$$V_{in} = \frac{V_{in1}}{m_{10}} - \frac{m_{20}}{m_{10}} V_{OS0}$$

$$V_{in1} = \frac{V_{in2}}{m_{11}} + d_1 V_{DAC1} \frac{m_{21}}{m_{11}} - \frac{m_{31}}{m_{11}} V_{OS1}$$

$$V_{in} = \frac{V_{in2}}{m_{10} m_{11}} + d_1 V_{DAC1} \frac{m_{21}}{m_{10} m_{11}} - \frac{m_{31}}{m_{10} m_{11}} V_{OS1} - \frac{m_{20}}{m_{10}} V_{OS0}$$

$$V_{in2} = \frac{1}{m_{12}} V_{in3} + d_2 V_{DAC2} \frac{m_{22}}{m_{12}} - \frac{m_{32}}{m_{12}} V_{OS2}$$

$$V_{in} = \frac{1}{m_{10} m_{11} m_{12}} V_{in3} + d_1 V_{DAC1} \frac{m_{21}}{m_{10} m_{11}} + d_2 V_{DAC2} \frac{m_{22}}{m_{10} m_{11} m_{12}} - \frac{m_{32}}{m_{10} m_{11} m_{12}} V_{OS2} - \frac{m_{31}}{m_{10} m_{11}} V_{OS1} - \frac{m_{20}}{m_{10}} V_{OS0}$$

• • •

Solution of the 2n linear equations

(Assuming for convenience that $m_{10}=1$, $V_{OS0}=0$)

$$V_{in} = \left\{ d_1 \left[\left(\frac{m_{21}}{m_{11}} \right) V_{DAC1} \right] + d_2 \left[\left(\frac{m_{22}}{m_{11}m_{12}} \right) V_{DAC2} \right] + \ldots + d_n \left[\left(\frac{m_{2n}}{m_{11}m_{12}\ldots m_{1n}} \right) V_{DACn} \right] \right\}$$

$$+ \left\{ \frac{m_{31}}{m_{11}} V_{OS1} + \frac{m_{32}}{m_{11}m_{12}} V_{OS2} + \ldots + \left(\frac{m_{3n}}{m_{11}m_{12}\ldots m_{1n}} \right) V_{OSn} \right\}$$

$$+ \left\{ \frac{V_{RESn}}{m_{11}m_{12}\ldots m_{1n}} \right\}$$

Solution of the 2n Linear Equations

$$V_{in} = \left\{ d_1 \left[\left(\frac{m_{21}}{m_{11}} \right) V_{DAC1} \right] + d_2 \left[\left(\frac{m_{22}}{m_{11}m_{12}} \right) V_{DAC2} \right] + \ldots + d_n \left[\left(\frac{m_{2n}}{m_{11}m_{12}\ldots m_{1n}} \right) V_{DACn} \right] + \frac{V_{REF}}{2^{n+1}} \right\}$$

Term involving digital output codes

$$+ \left\{ \frac{m_{31}}{m_{11}} V_{OS1} + \frac{m_{32}}{m_{11}m_{12}} V_{OS2} + \ldots + \left(\frac{m_{3n}}{m_{11}m_{12}\ldots m_{1n}} \right) V_{OSn} \right\}$$

Code-independent offset term

$$+ \left\{ \frac{V_{RESn}}{m_{11}m_{12}\ldots m_{1n}} - \frac{V_{REF}}{2^{n+1}} \right\}$$

Code-dependent but can be bounded by ½ LSB with out-range strategy

Note: Will not even include last residue amplifier nor create V_{RESn}

Note: ADC errors do not affect linearity performance of pipelined structure but DAC outputs and weights are critical

Solution of the 2n Linear Equations

$$V_{in} = \left[\sum_{k=1}^{n} d_k V_{DACk} \left(\frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \right) + \frac{V_{REF}}{2^{n+1}} \right] + \sum_{k=1}^{n} V_{OSk} \frac{m_{3k}}{\prod_{j=1}^{k} m_{1j}} + \left[\frac{V_{RESn}}{\prod_{k=1}^{n} m_{1k}} - \frac{V_{REF}}{2^{n+1}} \right]$$

If ADC is ideal (lets just verify):

$m_{ij} = 2$, $V_{DACk} = V_{REF}/2$, $V_{OSk} = 0$

$$V_{in} = \frac{V_{REF}}{2} \sum_{k=1}^{n} \frac{d_k}{2^{k-1}} + \frac{V_{REF}}{2^{n+1}} + \left(\frac{V_{RESn}}{2^n} - \frac{V_{REF}}{2^{n+1}} \right)$$

Performance is as expected

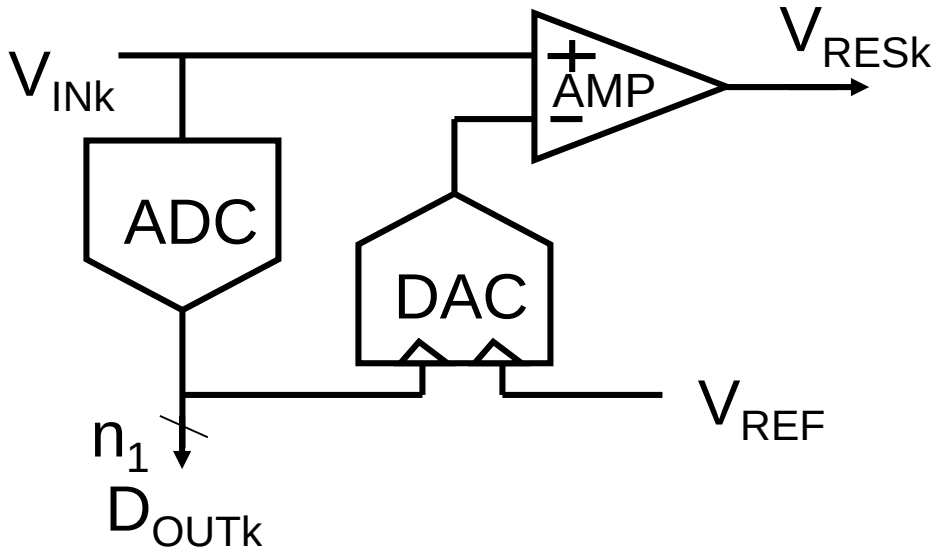
Solution of the 2n Linear Equations

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

$$\alpha_k = V_{DACk} \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}}$$

- **f(offset) is code-independent, ideally zero, and causes only overall offset error in ADC**
- **f(residue) is code-dependent but can be bounded by 1 lsb (causing at most ½ LSB error) with out-range protection**
- **No errors causing spectral distortion or INL degradation if α_k are correctly determined**

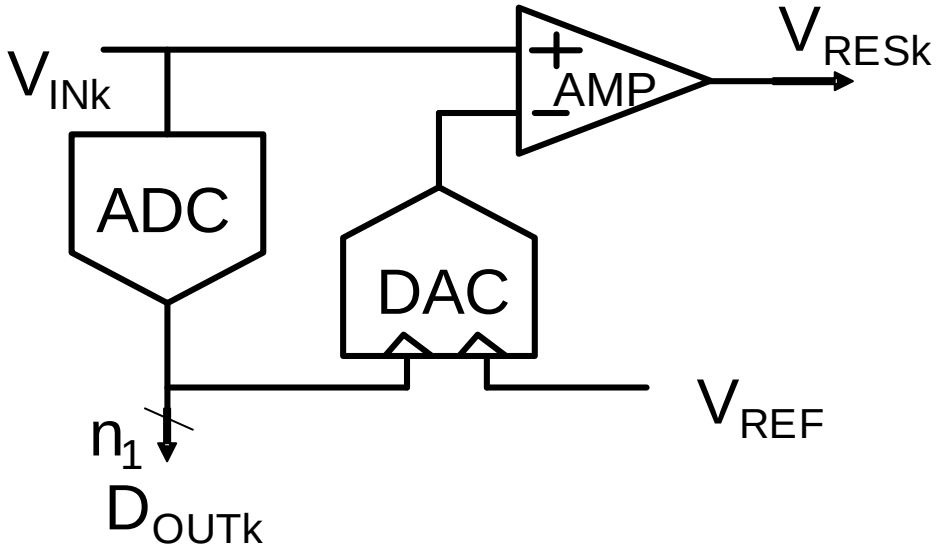
Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC



If more than 1 bit/stage is used and DAC is binarily-weighted structure

$$V_{RESk} = m_{1k} V_{ink} + m_{2k} \left(\sum_{j=1}^{2^{n_k}-1} d_{kj} V_{DACkj} \right) + m_{3k} V_{OSk}$$

Pseudo-Static Time-Invariant Modeling of a Linear Pipelined ADC



Or, in the most general case:

If DAC is characterized by $f_k\left(V_{REF}, \left\langle d_{kj} \right\rangle_{j=1}^{n_k}\right)$

$$V_{RESk} = m_{1k} V_{ink} + m_{2k}\left(f_k\left(V_{REF}, \left\langle d_{kj} \right\rangle_{j=1}^{n_k}\right)\right) + m_{3k} V_{OSk}$$

Solution of the 2n Linear Equations

If more than 1 bit/stage is used and DAC is binarily-weighted structure

$$V_{in} = \left[\sum_{k=1}^{n} \left(\sum_{j=1}^{h=n_{kj}} d_{kj} V_{DACkj} \right) \left(\frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \right) + \frac{V_{REF}}{2^{n+1}} \right] + \sum_{k=1}^{n} V_{OSk} \frac{m_{3k}}{\prod_{j=1}^{k} m_{1j}} + \left[\frac{V_{RESn}}{\prod_{k=1}^{n} m_{1k}} - \frac{V_{REF}}{2^{n+1}} \right]$$

If DAC is characterized by $f_k \left(V_{REF}, \left\langle d_{kj} \right\rangle_{j=1}^{n_k} \right)$

$$V_{in} = \left[\sum_{k=1}^{n} \left(f_k \left(V_{REF}, \left\langle d_{kj} \right\rangle_{j=1}^{n_k} \right) \right) \left(\frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}} \right) + \frac{V_{REF}}{2^{n+1}} \right] + \sum_{k=1}^{n} V_{OSk} \frac{m_{3k}}{\prod_{j=1}^{k} m_{1j}} + \left[\frac{V_{RESn}}{\prod_{k=1}^{n} m_{1k}} - \frac{V_{REF}}{2^{n+1}} \right]$$

No errors causing spectral distortion or INL degradation if terms involving d_{kj} are correctly determined

Pseudo-Static Characterization of Pipelined ADC with Arbitrary Bits/Stage and Out-Range Protection

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

- **d_k are boolean output variables from stage ADCs (including out-range protection if included)**
- **the α_k are functions of DAC levels and amplifier gains**
- **f(offset) is code-independent, ideally zero and causes only overall offset error in ADC**
- **f(residue) is code-dependent but can be bounded by 1 lsb (causing at most ½ LSB error) with out-range protection**
- **Equation applies to both sub-radix2 and extra comparator out-range protection**

•No errors causing spectral distortion or INL degradation if α_k are correctly determined

Observations

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

form of α_k : $V_{DACk} \frac{m_{2k}}{\prod_{j=1}^{k} m_{1j}}$

- Substantial errors are introduced if α_k are not correctly interpreted!
- Some calibration and design strategies focus on accurately setting gains and DAC levels
- Analog calibration can be accomplished with either DAC level or gain calibration
- Digital calibration based upon coefficient identification does not require accurate gains or precise DAC levels

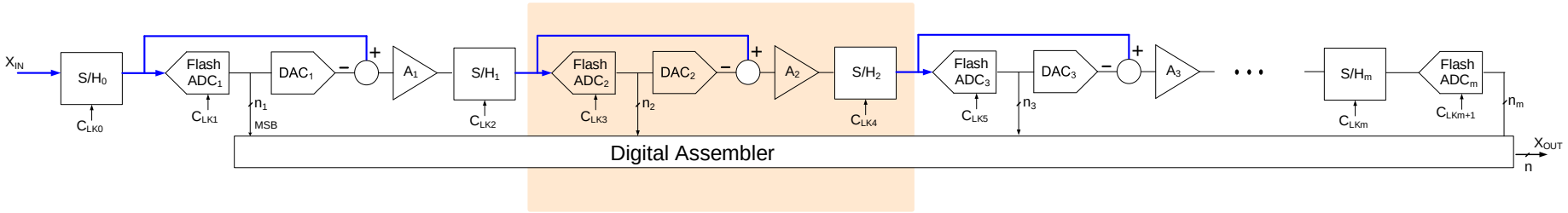
Observations (cont)

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

form of α_k : $V_{DACk} \dfrac{m_{2k}}{\prod_{j=1}^{k} m_{1j}}$

- If nonlinearities are avoided, data conversion process with a pipelined architecture is extremely accurate
- Major challenge at low frequencies is accurately interpreting the digital output codes

Pipelined ADC



Claim: If the Amplifiers are linear, settling is complete, and over-range protection is provided, the pipelined ADC makes no nonlinearity errors if the output of the DACs are correctly interpreted

Implication: Flash ADC errors, offsets in comparators and amplifiers, and gain errors in amplifier and S/H do not degrade linearity performance of a well-designed pipelined ADC structure !!

Observations (cont)

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

form of α_k : $V_{DACk} \dfrac{m_{2k}}{\prod_{j=1}^{k} m_{1j}}$

- If nonlinearities are present, this analysis falls apart and the behavior of the ADC is unpredictable !

Pseudo-Static Characterization of Pipelined ADC with Arbitrary Bits/Stage and Out-Range Protection

$$V_{in} = \sum_{k=1}^{n} \alpha_k d_k + f(\text{offset}) + f(\text{residue})$$

No errors causing spectral distortion or INL degradation if α_k are correctly determined and last residue is variability bounded

α_k terms are random variables at the design stage but deterministic at the chip level

f(residue) is random at the design stage but deterministic at the chip level

Key Questions:

How can the correct determination of the α_k terms be guaranteed ?

How can a required bound of f(residue) be achieved?

Approaches to Correctly Interpreting Output Codes

1. Design all components and blocks to be sufficiently ideal to achieve target performance with high yield
2. Reduce design requirements on components and blocks and use calibration (analog or digital) to achieve target performance with high yield
3. Try to achieve ideal performance and use calibration to overcome deficiencies in design

Which approach does industry almost exclusively follow today? **1**

Which approach shows the most promise for low voltage, high speed, high resolution design ? **2**

Why is approach 3 not the most attractive approach to follow ?

Can not derive enough speed and area benefits in emerging processes

(Remember assumption of linearity is still being made)

Stay Safe and Stay Healthy !

End of Lecture 23